The MR - - card is a gated single-shot trigger circuit that produces output pulses of a fixed time duration. The circuit consists of four PNP transistors and three capacitors of different values used in the time-out network. By changing the back panel wiring to the various capacitors on the card, different output pulse durations are possible. A positive shift to a gated input starts the single-shot action and provides a negative output pulse of a fixed time duration. This output pulse duration does not depend on the input staying up. A −S level at the gate input prevents the positive shift from starting the single-shot action. Additional control of the circuit is possible with a special hold input. This input can be used to initially start or maintain the single-shot active output (−S) regardless of the other input levels. The output remains active for the selected pulse duration after the hold input is released.

A typical application of the single-shot using an external timing capacitor is shown. Both the gate and hold inputs are returned to ground.

Circuit Description

With the input gate (pin N) at +S and the input hold (pin A) at +S, the status of the circuit is: T3 fully conducting, T2 and T7 partially conducting, T5 cut off, and output pin F at the +S level. The positive shift at input pin P, through the input capacitor and the input diode, reverse biases T3. T3 cuts off and T2 base seeks −12v. Output pin F falls to a −S level and T2 reaches full conduction. The negative shift at T2 emitter, through the selected timing capacitor and 150 ohm resistor, appears on the emitter of T7. T7 cuts off. This negative voltage shift, developed across the resistor network of 150 ohm, 5.1K, 13K,and the 15K potentiometer also appears at the base of T5. T5 base seeks the −4.2v and forward-biases the transistor on.

The positive shift at T5 collector is coupled back to T3 base, maintaining T3 cut off. This action is instantaneous through the coupling bypass capacitor C32. The circuit remains in this status while the timing capacitor charges through the resistor network toward +6v. As soon as T5 base reaches ground, T5 cuts off and the coupling voltage to T3 base is lost. The input shift has long since dissipated to ground through the input gate pin N. Therefore, T3 resumes conduction and output pin F rises to its former +S level. T2 and T7 resume partial conduction and the timing capacitor discharges through T7. The circuit is back to normal.

If the hold input is used, pin A is not returned to ground. An active output level can be maintained by establishing pin A at a −S level. T7 is biased to full conduction, lowering T5 base below ground; T5 conducts, and through the coupling to T3 base, T3 is cut off; and T2 goes to full conduction. Causing T7 to conduct drives the entire circuit to the same status as an input signal does. When the hold input is released (pin A rises to +S), the timing capacitor must again charge through the resistor network toward +6v. The output at pin F will remain active until T5 is cut off by the rise in its base level, and T3 again conducts.

The repetition rate of this circuit is 1.3 times the selected output pulse duration,if 0.3 of the output pulse duration is used for recovery of the circuit. Turn-off delays are a function of the input rise time, and circuit loading. Delay values vary from 0.16μs to 0.8μs.

Application

The pulse durations for the capacitor values on the single-shot card are summarized in the chart. An exact timing within the range noted is obtained by adjusting the 15K potentiometer. If additional timings are desired, external timing capacitor cards can be connected to the coupling pins. Refer to the MM - -, MN - -, and MP - - timing cards for other possible single shot timings.

Gate inputs are normally driven from CTRL logic circuits or from a voltage mode trigger. The gate input must be conditioned before the set input is applied. Levels and timings for the gated AC input operation are:

AC Set Input	Gate Level Before Conditioning	Gate Condition Time	Minimum Gate Level
6v	−12.48v	8.75μs	−0.5v
6v	−13.2v	8.90μs	−0.5v
6v	−6.24v	6.85μs	−0.5v
12v	−12.48v	5.00μs	−2.0v
12v	−13.2v	5.15μs	−2.0v