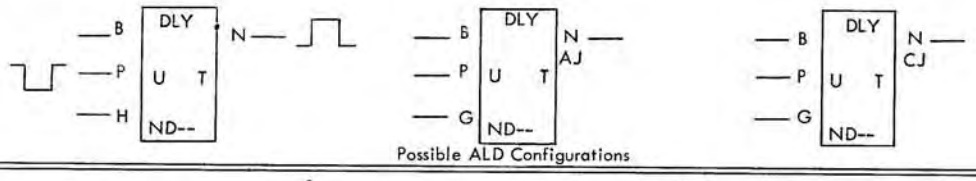
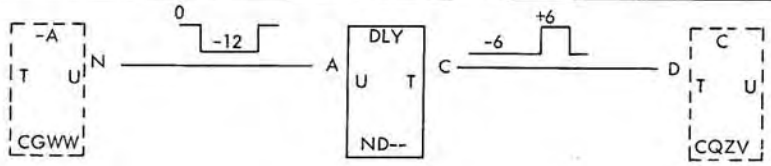
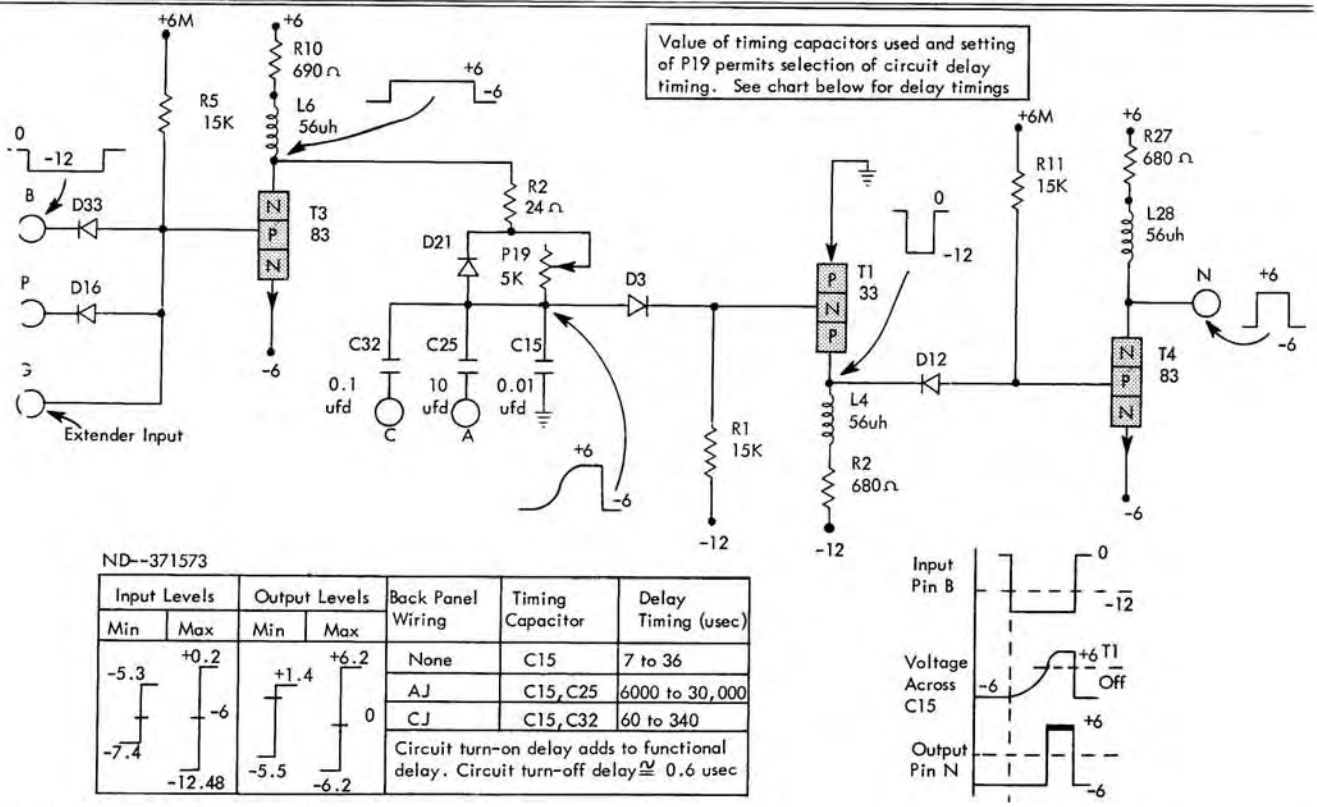


Possible ALD Configurations



Logic Application



ND--371573

Input Levels		Output Levels		Back Panel Wiring	Timing Capacitor	Delay Timing (usec)
Min	Max	Min	Max			
-5.3 to -7.4	+0.2 to -12.48	+1.4 to -5.5	+6.2 to -6.2	None	C15	7 to 36
				AJ	C15, C25	6000 to 30,000
				CJ	C15, C32	60 to 340
				Circuit turn-on delay adds to functional delay. Circuit turn-off delay ≅ 0.6 usec		

CTDL Universal Delay Circuit

The universal delay circuit provides an output pulse which begins at a definite time after the start of the input pulse. Only one delay circuit is on each card. The delay offered by the circuit is controlled by an RC network and is selected by back panel wiring to various capacitor values and by varying a 5K potentiometer.

A −U level at any of the input pins starts the delay timing and provides an out-of-phase T output. The output pulse duration is a function of the input signal duration and the circuit variables. This circuit is self-recycling, but requires a definite off period to insure the discharging of the timing capacitor(s).

Circuit Description (Circuit as Shown):

Assume all inputs in the up level; T3, T1, and T4 forward-biased and conducting. The CTDL output at pin N is near −6v and C15 is discharged to −6v through T3, R2, and the forward-biased D21.

When a −U level appears at pin B (or P or G), T3 is reverse-biased off and the collector of T3 increases to +6v. D21 is no longer forward-biased, so C15 must now charge through the 5K potentiometer, R2, L6, and R10 toward the +6v collector supply.

T1 remains in conduction until the charge on C15 is positive enough to reverse-bias T1. When T1 is cut off, its collector voltage drops to −12v and cuts off T4. The collector output of T4 increases toward +6v. This +T output (pin N) remains up until all inputs again are at the +U level. The RC charging time controls the cut off of T1 and delays the start of the positive output swing for the desired time interval.

Repetition Rate: The input must remain in the up level long enough to insure that the timing capacitor is fully discharged.

Application

The range of delay timings available for the various capacitor values used is noted in the chart. Specific timings within each range can be obtained by adjusting the 5K potentiometer. Loading considerations are similar to the standard CTDL logic block.