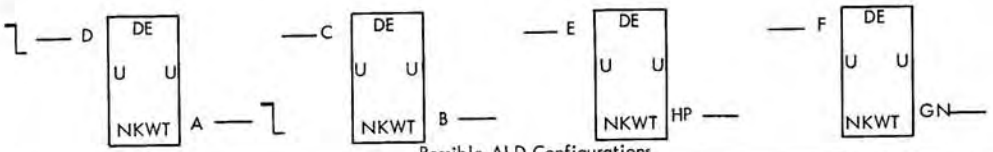
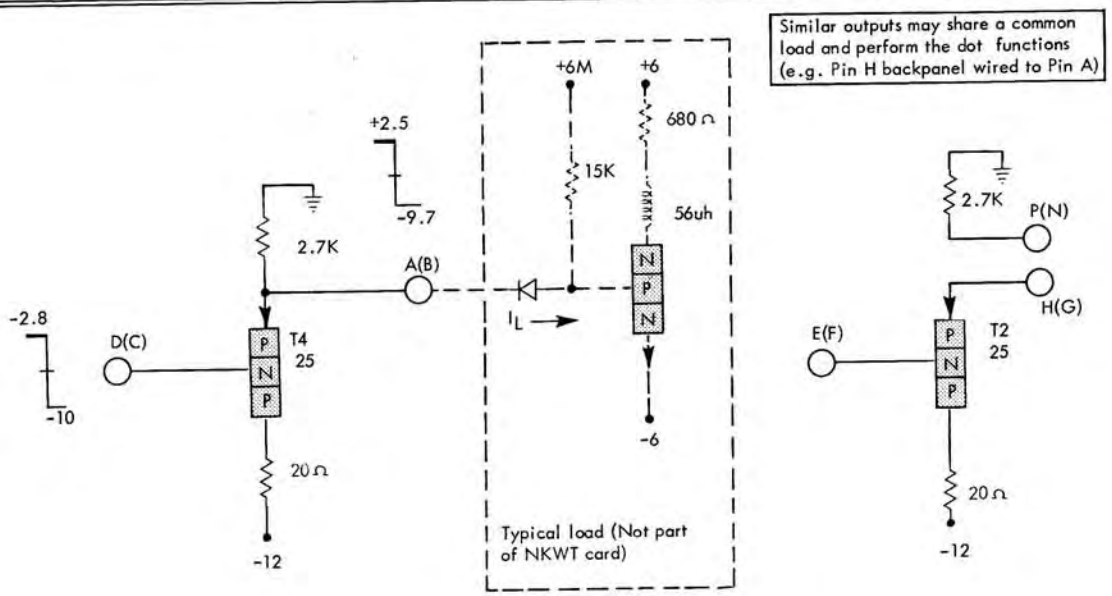


Possible ALD Configurations



Circuit 1 and 2

Circuits 3 and 4

NKWT 371631

Input Level		Output Level		Delays * (usec)				Circuit Use
Min	Max	Min	Max		Load	3 CTDL Blocks	15 CTDL Blocks	
-5.46 +0.24 -7.6 -6.74 -6		-5.2 +0.2 -7.4 -12.48 -6 -6		Turn On	Min	0.18	0.27	DE
					Max	0.48	0.62	-DEO
				Turn Off	Min	0.08	0.12	+DEA
					Max	0.17	0.33	

* Function of Capactive Loading and the Number of CTDL Blocks Driven

CTDL Emitter Follower PNP

The NKWT card consists of four one-way PNP emitter follower circuits that provide sufficient current to drive into branching circuits. Each circuit serves as a non-translating current amplifier, accepting a U input from CTDL logic blocks and providing an in-phase U output. A slight DC shift occurs between the input and output voltage levels. This card differs from the CPWT card in that 025 transistors are used instead of the 034 transistors. The 025 transistors have lower specifications than the 034.

Circuit Description

A +U line input allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value (minus the base-emitter drop of 0.3v). When the input drops to −10v, T4 is forward-biased more and conduction through T4 increases. The voltage at pin A follows the voltage swing at the base of T4 (minus the base-emitter drop). Typical loading is shown for the emitter follower. Capacitive loading and the number of blocks driven affect the circuit delays noted above.

Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use. The PNP emitter follower circuit is normally used for current amplification of negative going U lines and to furnish additional drive to P type branching circuits. These circuits are also used for impedance matching or for isolation without inversion.

Additional flexibility is provided on this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. For example, in the circuit illustrated above, the DEA function is performed if pin H is wired to Pin A. Considering positive logic, a +U input is required at both pins D and E to obtain a +U output at pin A and satisfy the DEA function. Circuits 3 and 4 also function as standard emitter followers by back-panel wiring to their respective emitter resistors.