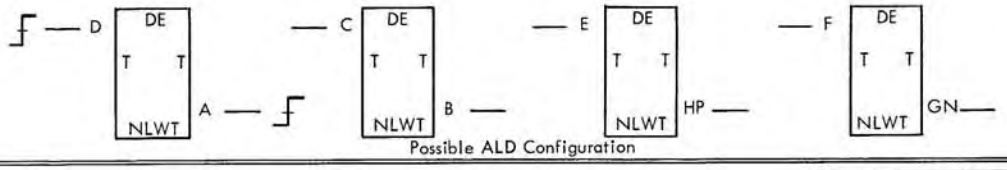
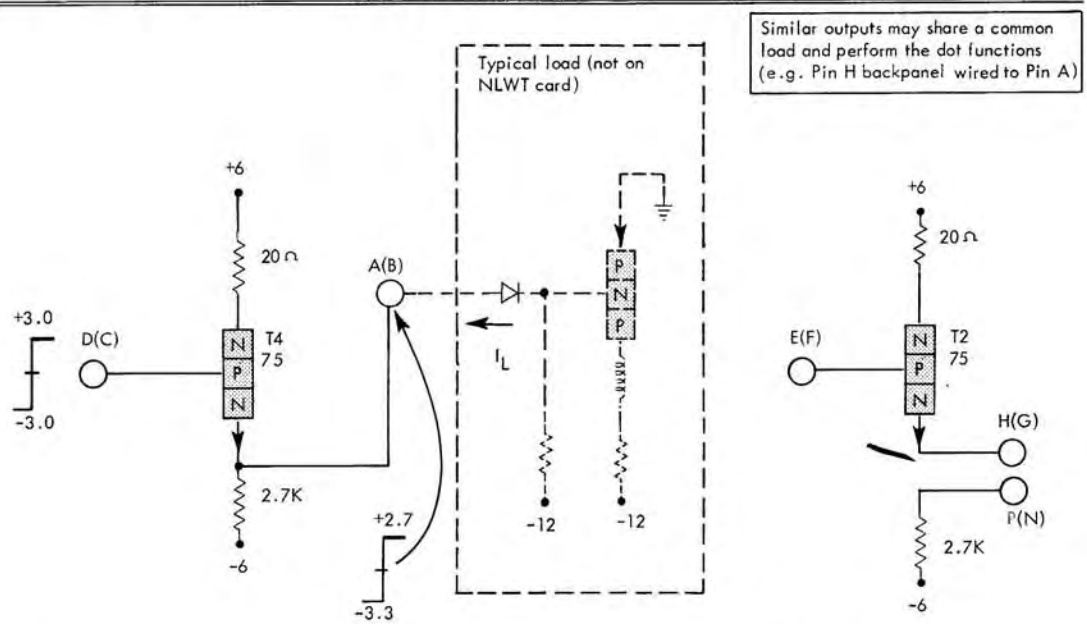


Possible ALD Configuration



Circuits 1 and 2

Circuits 3 and 4

NLWT--371632

Input Levels		Output Level		Delays * (usec)				Circuit Use
Min	Max	Min	Max		Load	3 CDTL Blocks	15 CTDL Blocks	
+1.8 to -0.7	+6.24 to -6.24	+1.44 to -0.7	+6.24 to -6.24	Turn On	Min	0.23	0.32	DE
					Max	0.68	0.68	-DEA
				Turn Off	Min	0.05	0.09	+DEO
					Max	0.13	0.25	

* Function of capacitive loading and number of CTDL blocks driven.

CTDL Emitter Follower NPN

The NLWT card consists of 4 one-way NPN emitter follower circuits that provide sufficient current to drive into branching circuits. Each circuit serves as a non-translating current amplifier that accepts a T input from a CTDL logic block and provides an in-phase T output. A slight DC shift occurs between the input and output voltage levels. This card differs from the CNWT card in that 075 transistors are used instead of the 083 transistors. The 075 transistors have lower specifications than the 083.

Circuit Description

A-T level input allows a minimum of current to flow through the emitter follower T4. The output at pin A clamps to this input value (minus the base-emitter voltage drop of approximately 0.3v). When the input increases to +3v, conduction through T4 increases and the output at pin A clamps to the input voltage. Typical loading is noted above for the emitter follower. Capacitive loading and the number of blocks driven affect the circuit delays.

Application

The logical functions performed by these circuits are indicated by the symbols listed in the chart labeled Circuit Use.

These circuits are normally used for power amplification of positive-going T lines, for impedance matching, or for isolation without inversion of a signal.

Additional flexibility is provided by this card for performing the DOT functions. With the emitters of circuits 3 and 4 returned to terminal pins, connections for sharing a common emitter load are easily made by back-panel wiring. For example, in the circuits illustrated above, the DEO function is performed if pin H is wired to pin A. Considering positive logic, a +T input at either pin D or pin E will give a +T output at pin A, and satisfy the DEO function. Circuits 3 and 4 can also function as standard emitter followers by back-panel wiring to their respective emitter resistors.