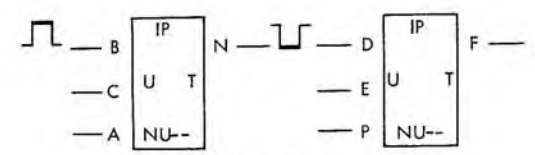
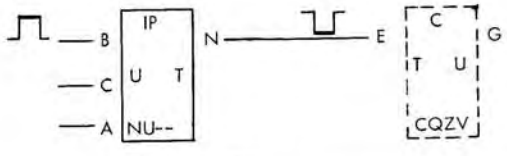
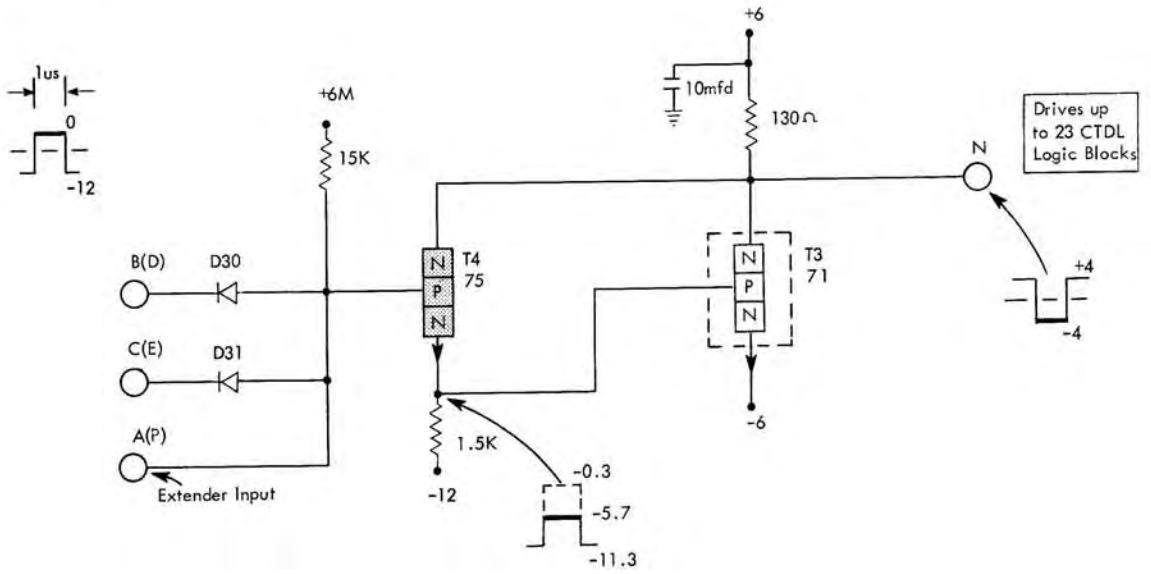


Possible ALD Configurations



Logic Application



Input Levels		Output Levels		Delays (usec)			Output Current	
Min	Max	Min	Max					
-4.65 to -7.44	+2.4 to -12.48	+1.44 to -5.46	+6.24 to -6.24	Turn On	Min	0.09	Up Level	Down Level
					Max	0.38		
				Turn Off	Min	0.11	23.5 ma	4.5 ma
					Max	0.13		

CTDL Power Inverter

The NU--card consists of two power inverter circuits capable of driving 23 CTDL logic blocks. Each circuit is basically a modified emitter follower driving an inverter. A relatively small input signal develops a large power output for driving into the CTDL loads. The input circuit is similar to the CTDL logic block and has two diode inputs and an extender input. A +U line of at least 1μs duration at all inputs is required to drive T4 into maximum conduction and provide a −T output from T3.

Circuit Description

When any of the inputs at pins A, B, or C are down (−U level), minimum current flows through the 1.5K resistor and the emitter follower T4. The emitter follower output holds T3 off and only the small current flow from T4 flows through the 130 ohm resistor. A +T output exists at pin N.

Coincidence of +U levels at all the input pins causes T4 to become more forward-biased. Increased current flow through the 1.5K emitter resistor, T4, and the 130 ohm resistor to +6v causes the base of T3 to rise above −6v. T3 becomes forward-biased on. When T3 turns on, additional current through the 130 ohm resistor quickly drops the output at pin N to a −T level. At this time up to 30ma is supplied.

The 130 ohm resistor relates the two collectors so that if T3 tends to become saturated, the current through T4 is decreased, which in turn reduces the base current to T3. This degenerative action prevents T3 from operating in saturation and provides medium current outputs with minimum turn-on and turn-off delays.

Application

Typical loading is shown in the circuit.