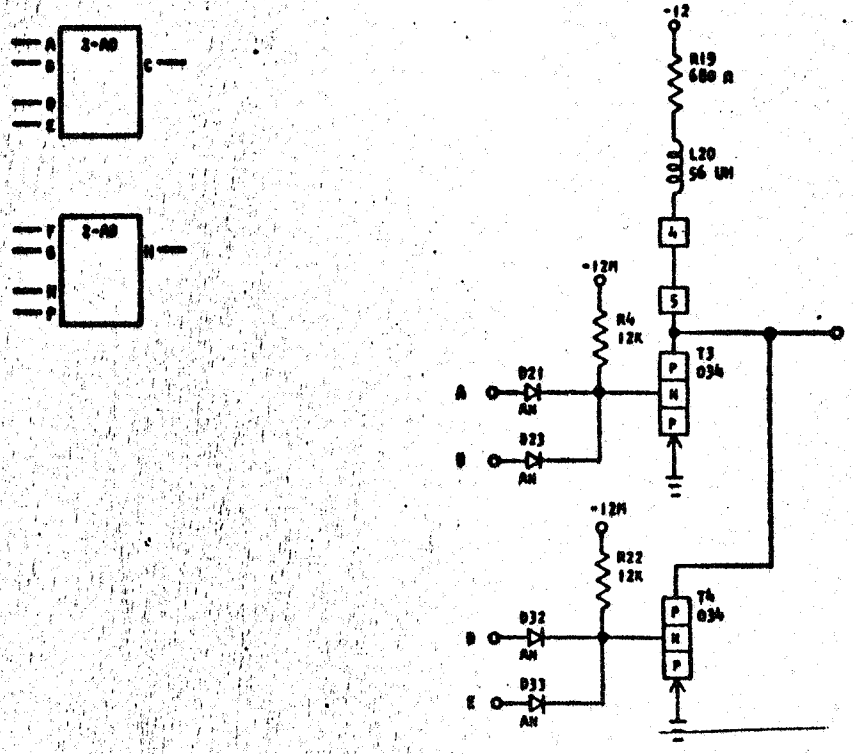
729900

CARD CODE	729900
4J MX	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370142

CTDL PNP TWO WAY GATE WITH COLLECTOR LOAD



SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR DOWN, TRANSISTOR ON OUTPUT UP
2. FOR DOWN OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE UP
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

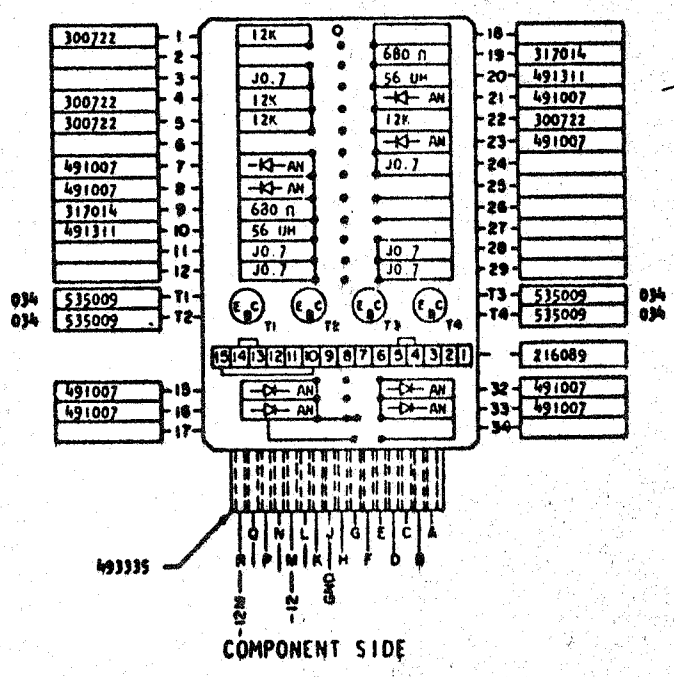
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,F B,N	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
B,G E,P	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,M	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL PNP					6-19-62	EC 115599					729900
TWO WAY GATE WITH COLLECTOR LOAD						10-4-63	TT83687					
DESIGN			MODEL	SMS								
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LTG	3-17-62							
APPRO			CHECK									

C

729900