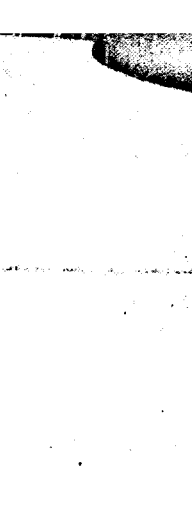
STANDARDS CODE
729842

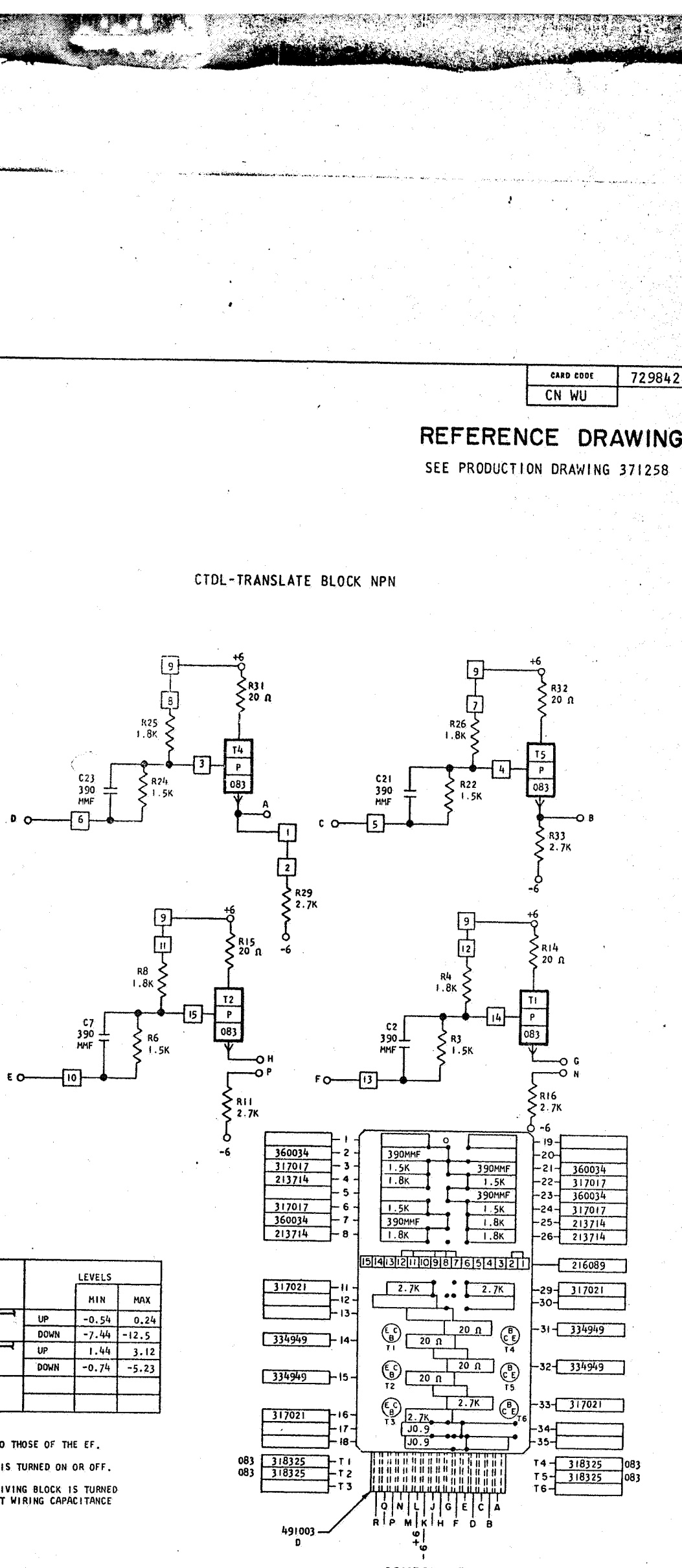
CARD CODE	729842
CN WU	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371258

CTDL-TRANSLATE BLOCK NPN





COMPONENT SIDE

SEQUENCE OF OPERATION

1. TRANSISTOR ALWAYS IN CONDUCTION; T1, T2, EMITTER MUST BE LOADED
2. OUTPUT WILL FOLLOW INPUT
3. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D,C, E,F	U	INPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5
A,B, H,G	T	OUTPUT		UP	1.44	3.12
				DOWN	-0.74	-5.23

DELAY

THE DELAY CHARACTERISTICS OF THE TRANSLATE BLOCK ARE SIMILAR TO THOSE OF THE EF.

NO APPRECIABLE DELAY SHOULD BE NOTICED WHEN THE DRIVING BLOCK IS TURNED ON OR OFF.

APPRECIABLE DELAY CAN BE OBSERVED (1 TO 2.5 USEC.) WHEN THE DRIVING BLOCK IS TURNED ON AND THE OUTPUT OF THE TRANSLATE BLOCK IS DRIVING SIGNIFICANT WIRING CAPACITANCE (SEVERAL FEET OF WIRE FROM ONE GATE TO ANOTHER.)

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR - CTDL TRANSLATE BLOCK NPN					-62	115599						729842
DESIGN			MODEL	SMS									
DETAIL	RQ	3-1-62	SCALE	NONE									
CHECK	WH	3-1-62	DRAW	LIC	3-17-62								
APPRO			CHECK										

C