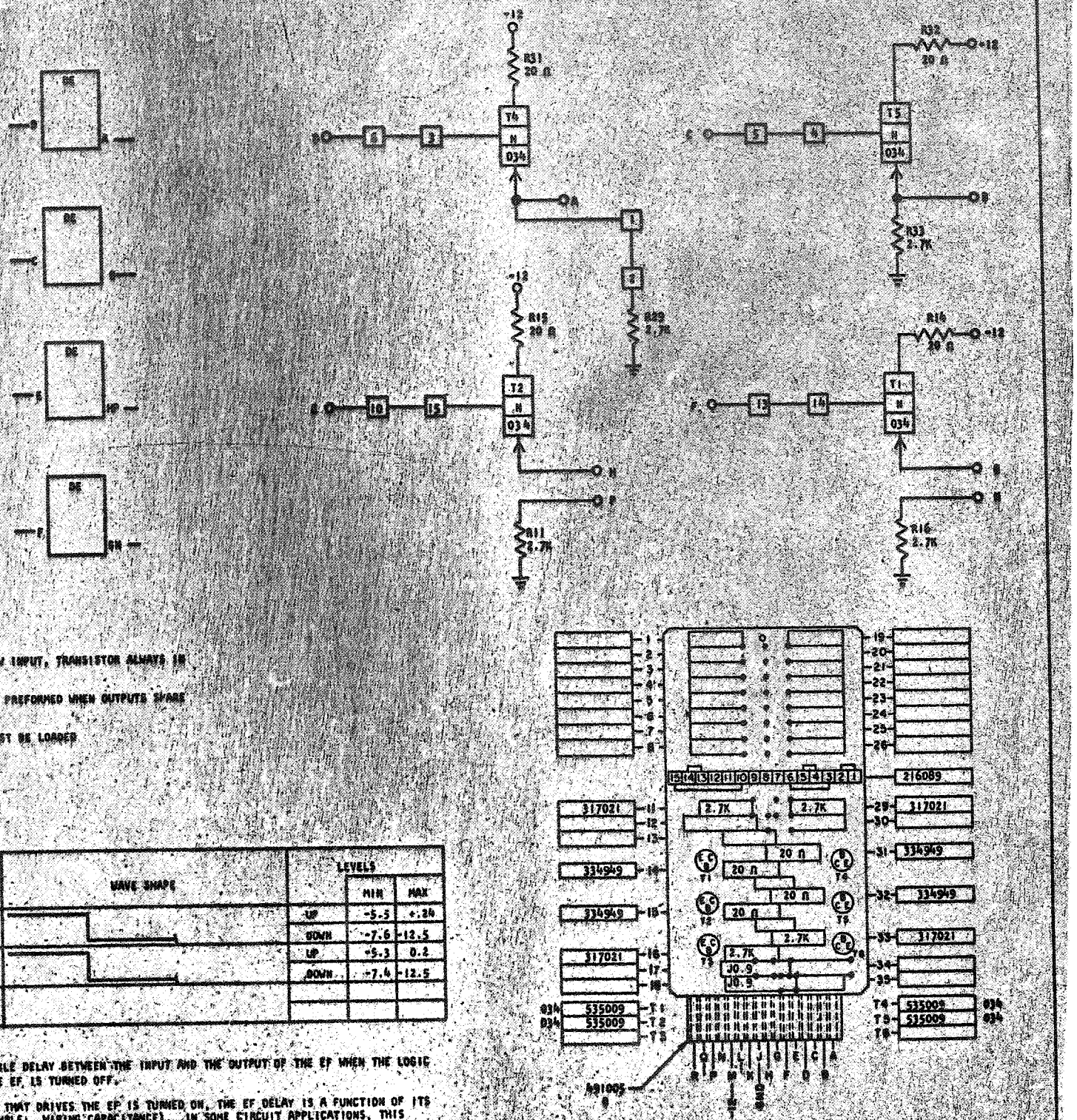
CARD CODE	729843
CP WT	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371259

CTDL - EMITTER FOLLOWER PNP



SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT, TRANSISTOR ALWAYS IN CONDUCTION
2. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD
3. T1, T2 EMITTER MUST BE LOADED

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D, C, E, F	U	INPUT		UP	-5.5	+.24
				DOWN	-7.6	-12.5
A, B, H, G	U	OUTPUT		UP	-5.3	0.2
				DOWN	-7.4	-12.5

DELAY

THERE IS NO APPRECIABLE DELAY BETWEEN THE INPUT AND THE OUTPUT OF THE EF WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED OFF.

WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED ON, THE EF DELAY IS A FUNCTION OF ITS CAPACITIVE LOAD (EXAMPLE: WIRING CAPACITANCE). IN SOME CIRCUIT APPLICATIONS, THIS DELAY CAN BE IN THE ORDER OF 3 OR 4 USEC. IN NORMAL APPLICATION (NO APPRECIABLE WIRING CAPACITANCE ON THE OUTPUT OF THE EF) THE DELAY IS NOT APPRECIABLE.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR - CTDL EMITTER FOLLOWER PNP					6-29-62	EC 115599					
						10-4-62	JT 83689					
DESIGN			MODEL	SMS								
DETAIL	RG	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPROV			CHECK									

729843

C