

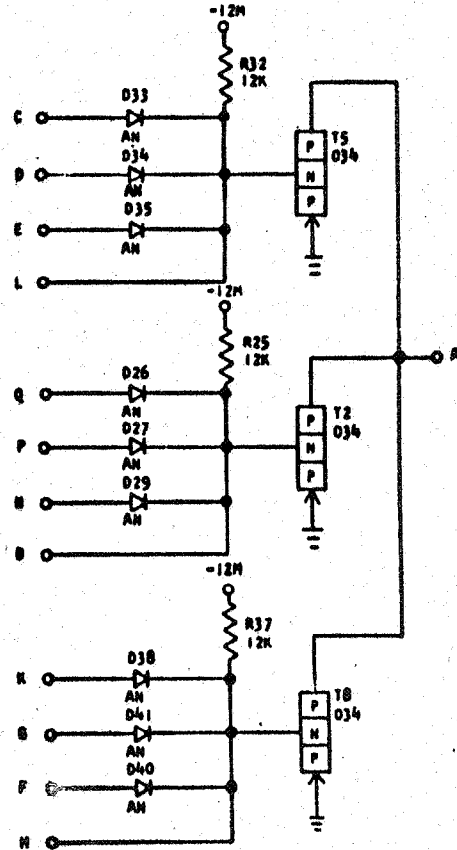
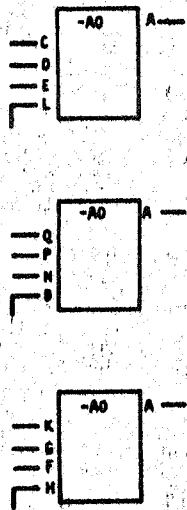
729816

STANDARD CODE

CARD CODE 729816  
CEE -

REFERENCE DRAWING  
SEE PRODUCTION DRAWING 370140

CTDL PNP-3 WAY AND GATE



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTOR LOADING REQUIRED
4. INPUTS ON EXTENDER CARD MUST BE DOWN IN COINCIDENCE WITH INPUTS ON CARD FOR UP OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

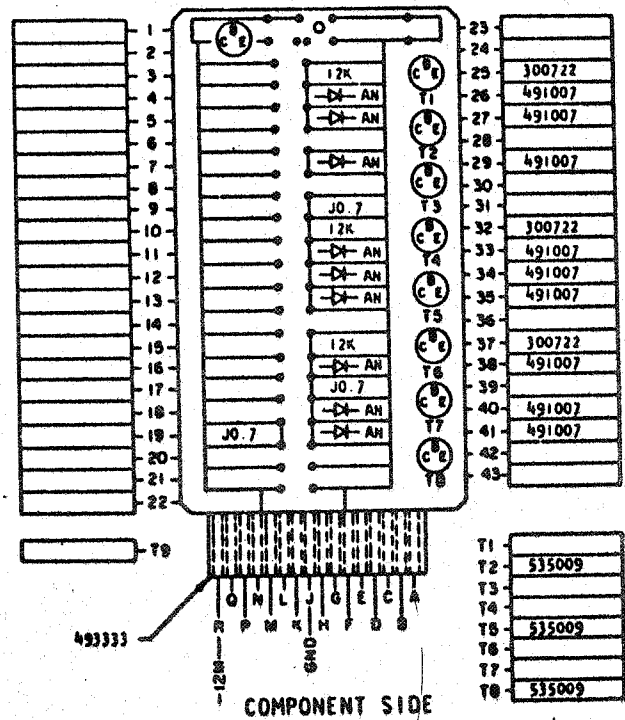
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS		
			MIN	MAX	
C, D, E	T INPUT	[Waveform: High to Low]	UP	1.44	6.24
			DOWN	-0.74	-6.24
Q, P, N	T INPUT	[Waveform: High to Low]	UP	1.44	6.24
			DOWN	-0.74	-6.24
K, G, F	T INPUT	[Waveform: High to Low]	UP	1.44	6.24
			DOWN	-0.74	-6.24
L, O, H	EXTENDER INPUT	[Waveform: High to Low]	UP	1.44	6.24
			DOWN	0	0
A	U OUTPUT	[Waveform: Low to High]	UP	-0.54	0.24
			DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

\*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING FF 'OR'.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR -CTDL PNP 3	DATE	4-2-62	CHANGE NO.	EC115599	APPROVAL		DATE		DEVELOPMENT NO.
DESIGN	WAY AND GATE	DATE	30-4-63	CHANGE NO.	JT 83687	APPROVAL		DATE		DEVELOPMENT NO.
DETAIL	RQ 3-1-62	SCALE	NONE							
CHECK	VM 3-1-62	DRAW	LIG 3-17-62							
APPRO		CHECK								

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