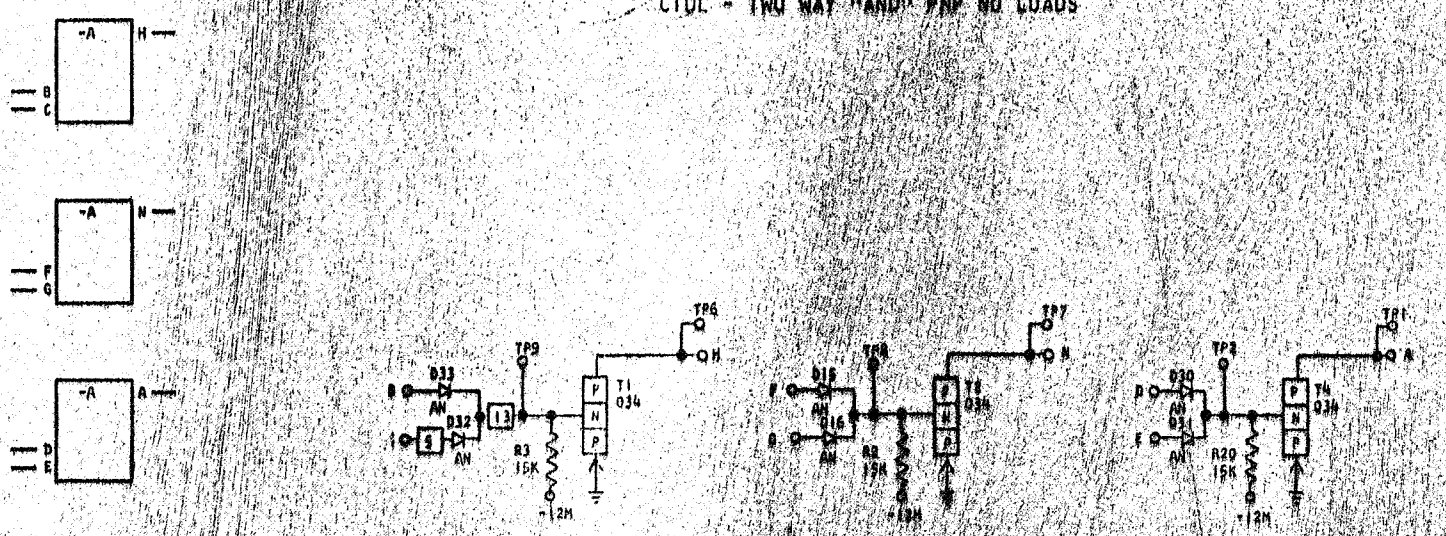
STANDARDS CODE 729820

CARD CODE 729820
CG - - -

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371263

CTDL - TWO WAY "AND" PNP NO LOADS



SEQUENCE OF OPERATION

1. BOTH INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. EXTERNAL COLLECTOR LOADING REQUIRED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

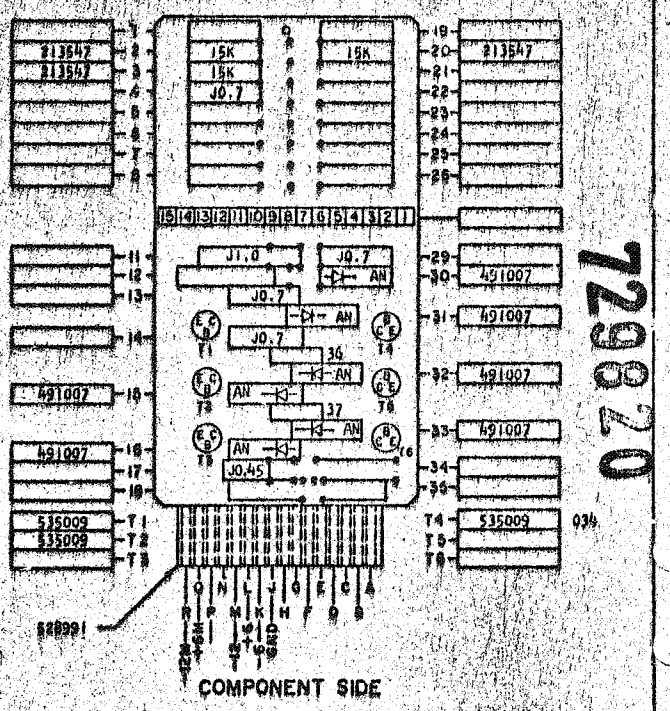
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B,F,D	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,G,E	T	INPUT *		UP	1.44	6.24
				DOWN	-0.74	-6.24
H,N,A	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

* DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



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CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM FSTR -CTDL - TWO WAY "AND" PNP NO LOADS				6-1-62	115099					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRD			CHECK								

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C