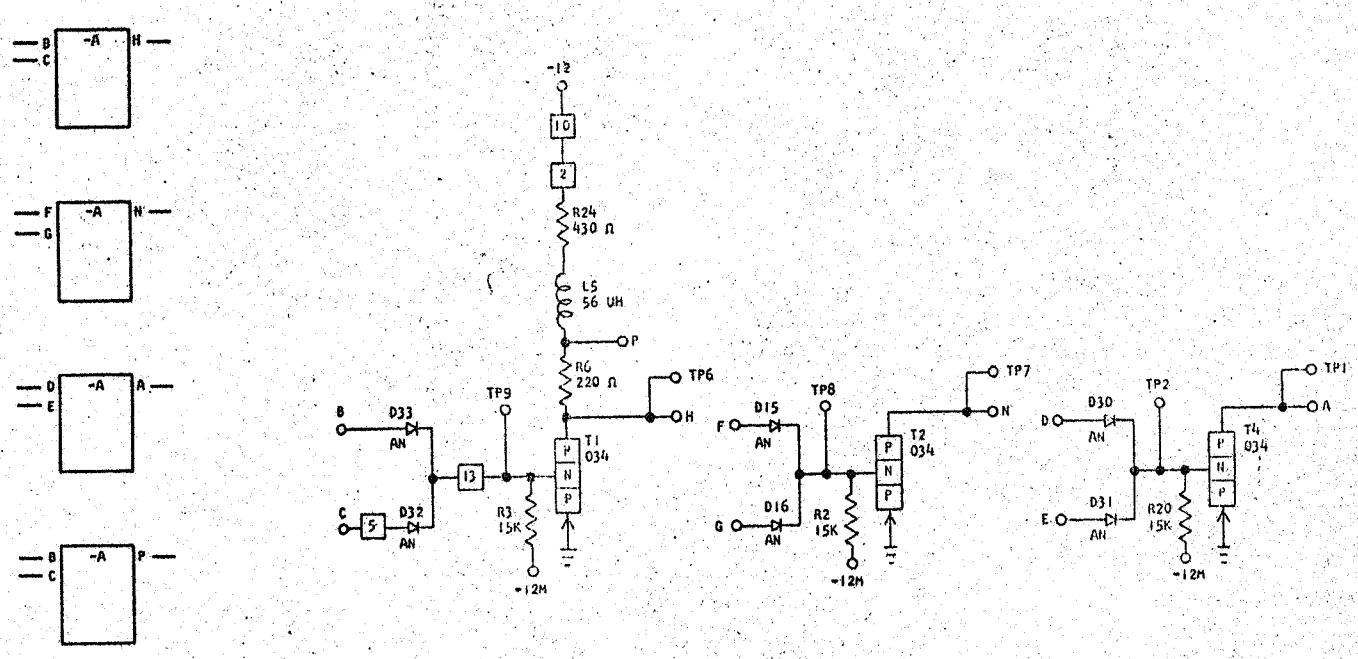
STANDARDS CODE	CARD CODE	729821
729821	CG VV	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371262

CTDL - TWO WAY "AND" PNP ONE LOAD



SEQUENCE OF OPERATION

1. BOTH INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. T2, T4, COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

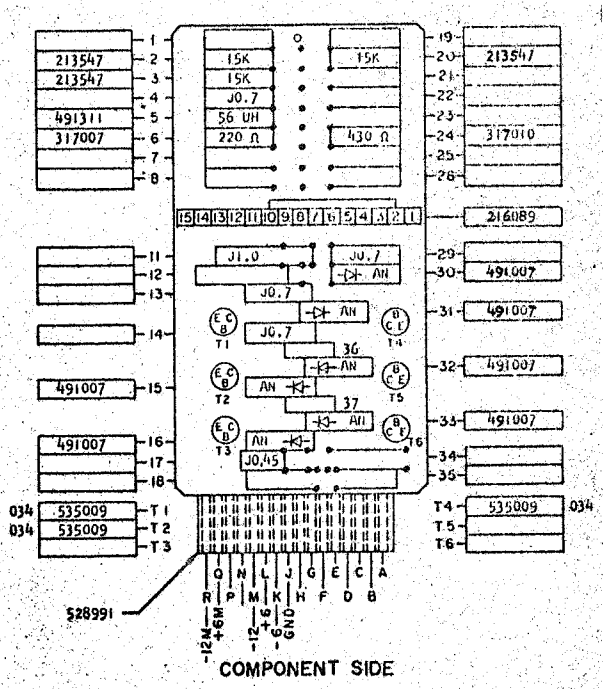
PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
B,F,D	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
C,G,E	T	INPUT		UP	1.44	6.24
				DOWN	0.74	-6.24
H,N,A	U	OUTPUT		UP	0.54	0.24
				DOWN	-7.44	-12.5
P	P	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR -CTDL - TWO WAY "AND" PNP ONE LOAD					-62	115599					
DESIGN			MODEL	SMS								
DETAIL	RO	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

729821

C

729821