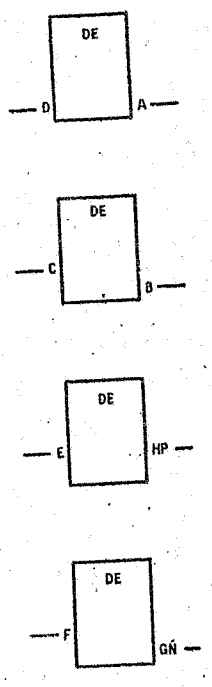
CARD CODE	729841
CN WT:	

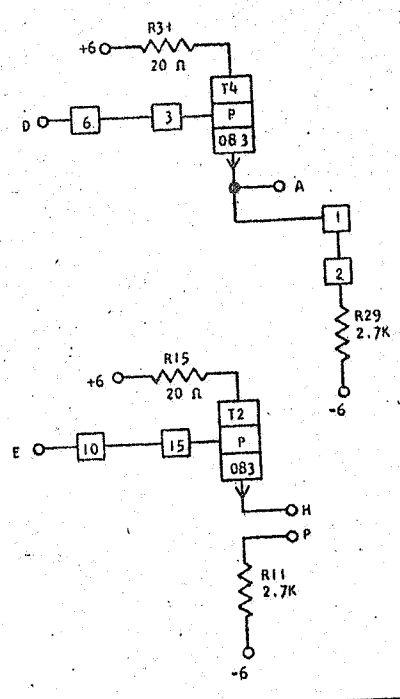
STANDARDS CODE 729841

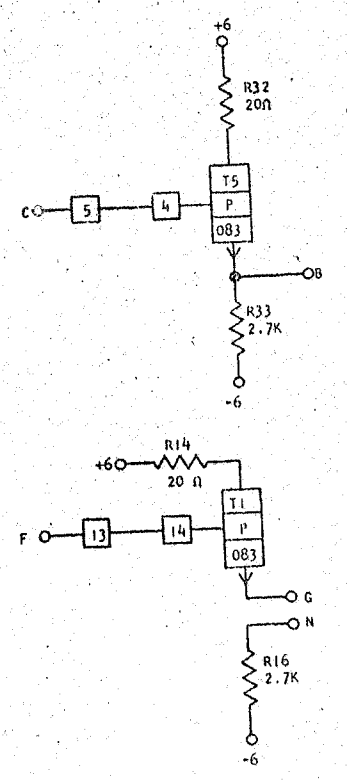
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371260

CTDL - EMITTER FOLLOWER NPN







SEQUENCE OF OPERATION

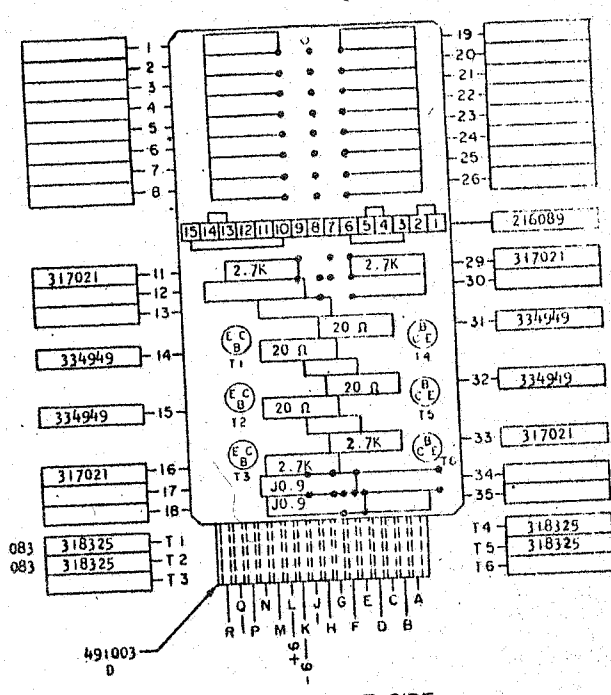
1. OUTPUT WILL FOLLOW INPUT, TRANSISTOR ALWAYS IN CONDUCTION
2. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD
3. T1, T2, EMITTER MUST BE LOADED

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C, D E, F	T	INPUT		UP	1.9	6.24
				DOWN	-5.46	-6.24
A, B H, P	T	OUTPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24

DELAY

THESE IS NO APPRECIABLE DELAY BETWEEN THE INPUT AND THE OUTPUT OF THE EF WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED OFF.

WHEN THE LOGIC BLOCK THAT DRIVES THE EF IS TURNED ON, THE EF DELAY IS A FUNCTION OF ITS CAPACITIVE LOAD (EXAMPLE: WIRING CAPACITANCE). IN SOME CIRCUIT APPLICATIONS, THIS DELAY CAN BE IN THE ORDER OF 3 OR 4 USEC. IN NORMAL APPLICATION (NO APPRECIABLE WIRING CAPACITANCE ON THE OUTPUT OF THE EF) THE DELAY IS NOT APPRECIABLE.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO
NAME	CARD ASM TSTR - CTDL EMITTER FOLLOWER NPN				4-6-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			SMS CA								

C

729841