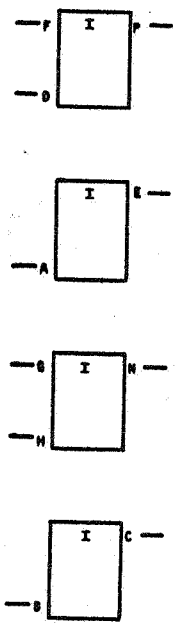
729880 STANDARDS CODE

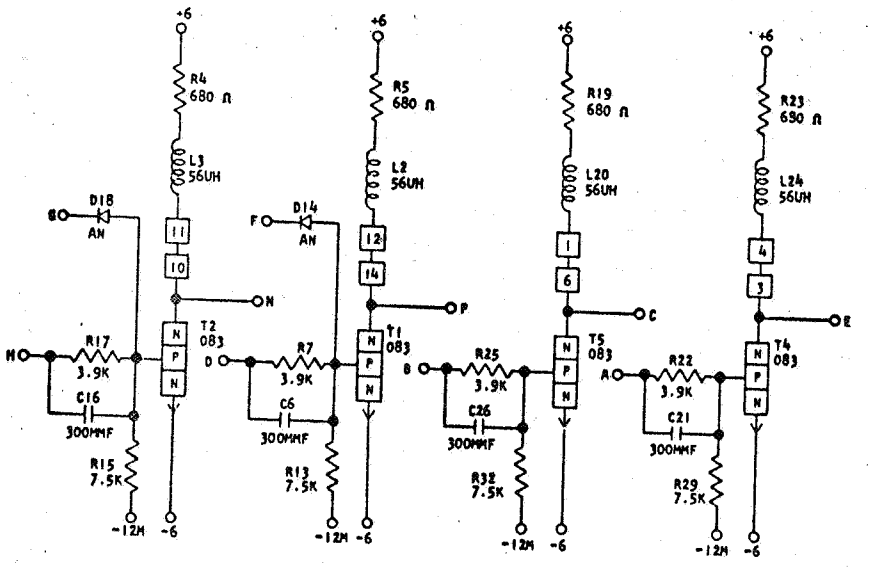
CARD CODE	729880
JM V8	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371079

CTDL LOGIC INVERTER NPN ALL LOADS





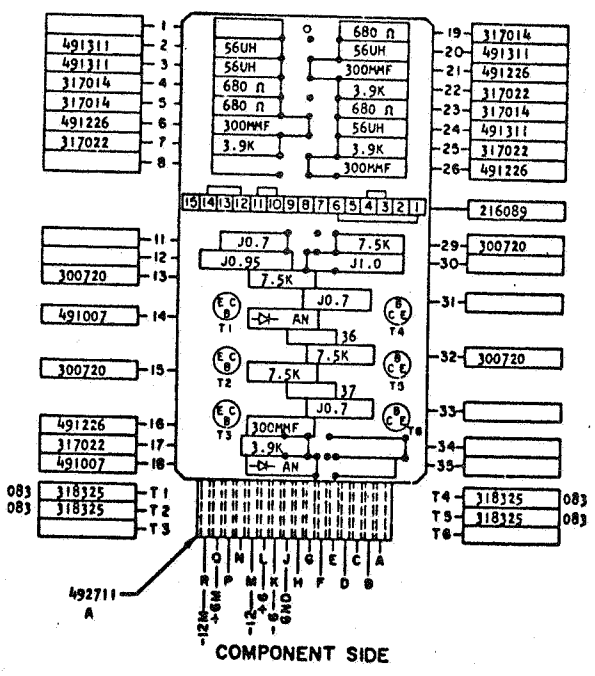
SEQUENCE OF OPERATION

1. GATE AND SIGNAL UP, TRANSISTOR ON, DOWN OUTPUT.
2. GATE OR SIGNAL DOWN, TRANSISTOR OFF, UP OUTPUT.
3. INPUT DOWN, TRANSISTOR OFF, OUTPUT UP.
4. INPUT UP, TRANSISTOR ON, OUTPUT DOWN.
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,D	T	INPUT SIGNAL		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
G,F	U	INPUT GATE		UP	-5.26	+0.24
				DOWN	-7.44	-12.48
N,P	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
B,A	T	INPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24
C,E	T	OUTPUT		UP	+1.44	+6.24
				DOWN	-5.46	-6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	-0.05	0
TURN OFF	-0.05	+0.40



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL LOGIC INVERTER NPN ALL LOADS					4-24-62	EC 115599					729880
DESIGN			MODEL	SMS		30-4-63	JT 83687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C