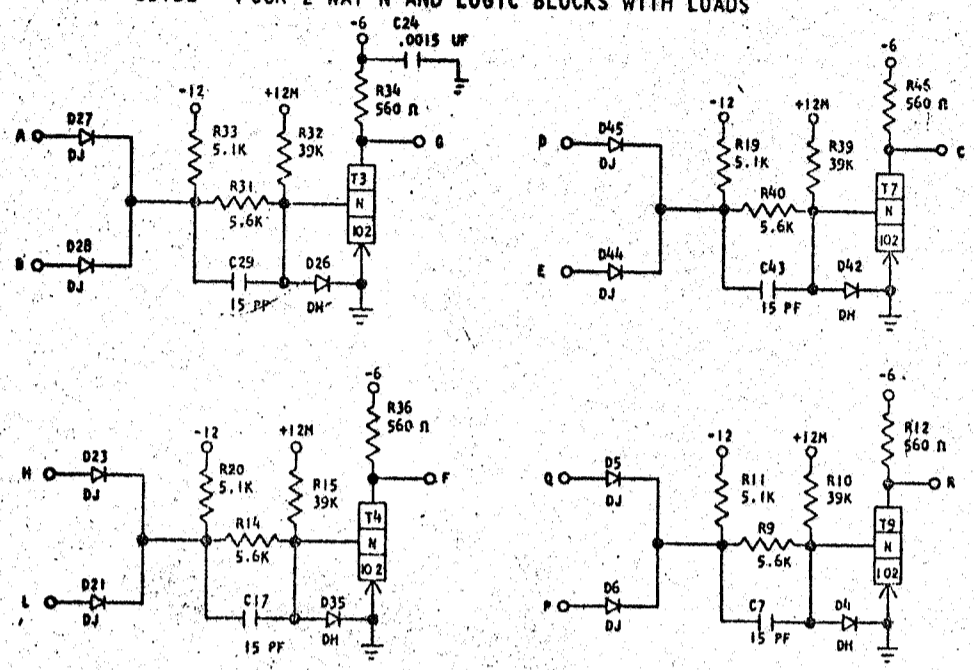
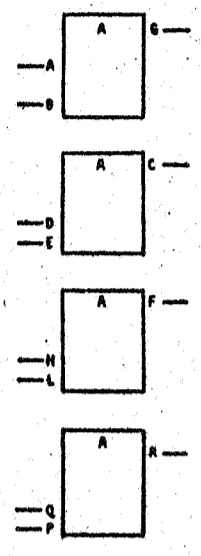


STANDARDS CODE
729906

CARD CODE
DEF - 729906

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370216

SDTDL - FOUR 2 WAY N AND LOGIC BLOCKS WITH LOADS



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

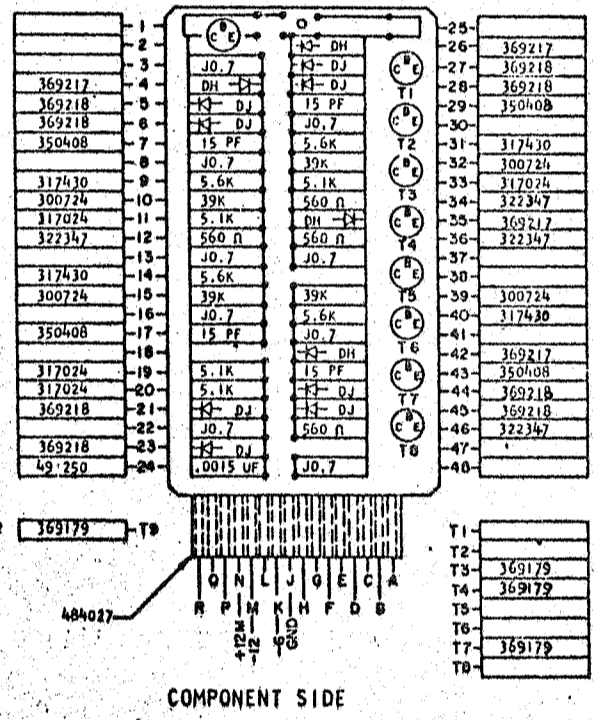
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
A, D, H, Q	Y INPUT	[Waveform: High then Low]	UP	-0.65 - -1
B, E, L, P	Y INPUT	[Waveform: High then Low]	DOWN	-5.81 - -8.8
G, F, R, S	Y OUTPUT	[Waveform: High then Low]	UP	-0.65 - -1
			DOWN	-5.81 - -8.8

DELAY: SDTDL - HIGH SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	5	30*
TURN OFF (NSEC)	10	80**

- *THIS DELAY CAN INCREASE TO 75 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.
- **THIS DELAY CAN INCREASE TO 120 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM ISTR-SDTDL-FOUR				4-2-62	EC 115599					729906
2-WAY N AND LOG BCKS WITH LOADS				30.4.63	JY 83687					
DESIGN		MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE						
CHECK	WH	3-1-62	DRAW	LIG	3-17-62					
APPRO			CHECK							

729906

C

4