

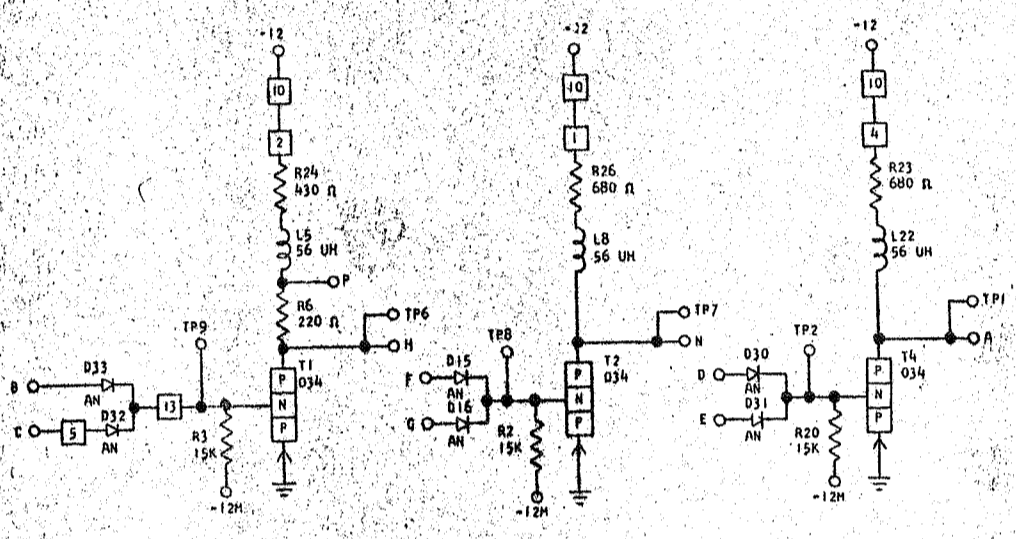
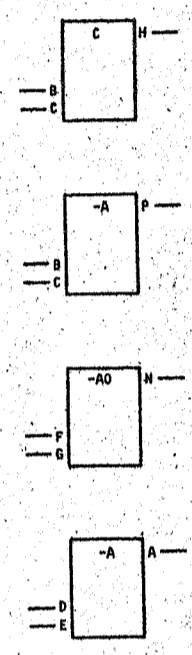
729823

STANDARDS CODE

CARD CODE 729823
CG WW

REFERENCE DRAWING
SEE PRODUCTION DRAWING 371251

CTDL - TWO WAY "AND" PNP



SEQUENCE OF OPERATION

1. BOTH INPUTS DOWN, TRANSISTOR ON, OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

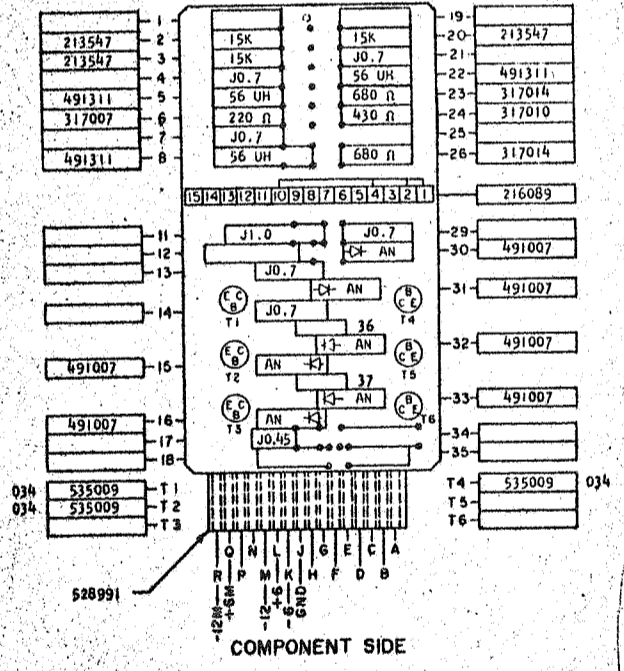
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
B, F, D	T	INPUT	UP	1.44 - 6.2
			DOWN	-0.7 - -6.2
C, G, E	T	INPUT	UP	1.44 - 6.2
			DOWN	-0.7 - -6.2
H, N, A	U	OUTPUT	UP	-0.5 - 0.2
			DOWN	-7.4 - -12.5
P	P	OUTPUT	UP	-4.93 - -3.54
			DOWN	-8.82 - -12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EP 'ON'.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM	TSTR-CTRL - TWO	WAY "AND" PNP	62	115599					
DESIGN	RQ	3-1-62	SCALE	NONE						
DETAIL	WH	3-1-62	DRAW	L16	3-1-62					
CHECK										
APPRO										

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