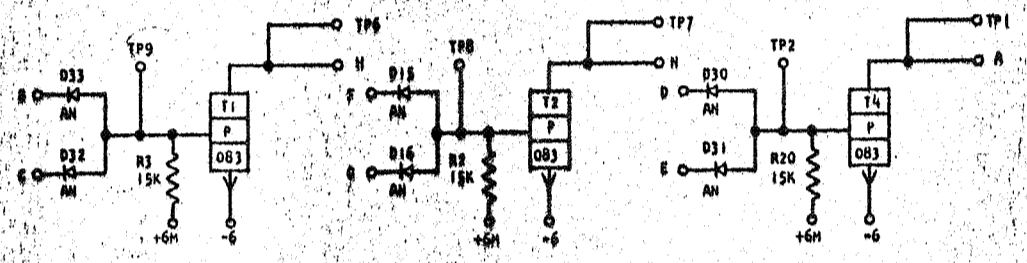
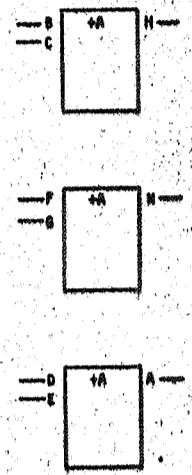


STANDARD CODE
729824

CARD CODE 729824
CH --

REFERENCE DRAWING
SEE PRODUCTION DRAWING 371266

CTDL - TWO WAY "AND" NPN NO LOADS



SEQUENCE OF OPERATION

1. BOTH INPUTS UP, TRANSISTOR ON, OUTPUT DOWN
2. ANY INPUT DOWN, TRANSISTOR OFF, OUTPUT UP
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

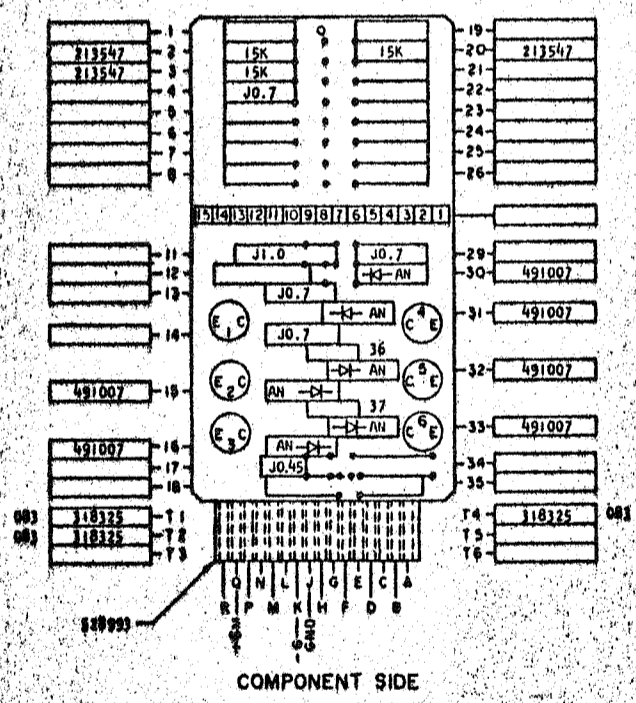
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
B, F, D	U INPUT	[Waveform: High then Low]	UP	-5.26 0.24
			DOWN	-7.44 -12.5
C, G, E	U INPUT	[Waveform: High then Low]	UP	-5.26 0.24
			DOWN	-7.44 -12.5
H, A, A	T OUTPUT	[Waveform: Low then High]	UP	1.44 6.24
			DOWN	-5.46 -6.24

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING OF "OR".



CIRCUIT AND PACKAGING STANDARD

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR - CTDL-TWO				4-2-62	115899					729824
WAY "AND" NPN NO LOADS										
DESIGN	NO	MODEL	SPS							
DETAIL NO	3-1-62	SCALE	NONE							
CHECK NO	3-1-62	DRAW	LIG D-17-62							
APPROV		CHECK								

729824