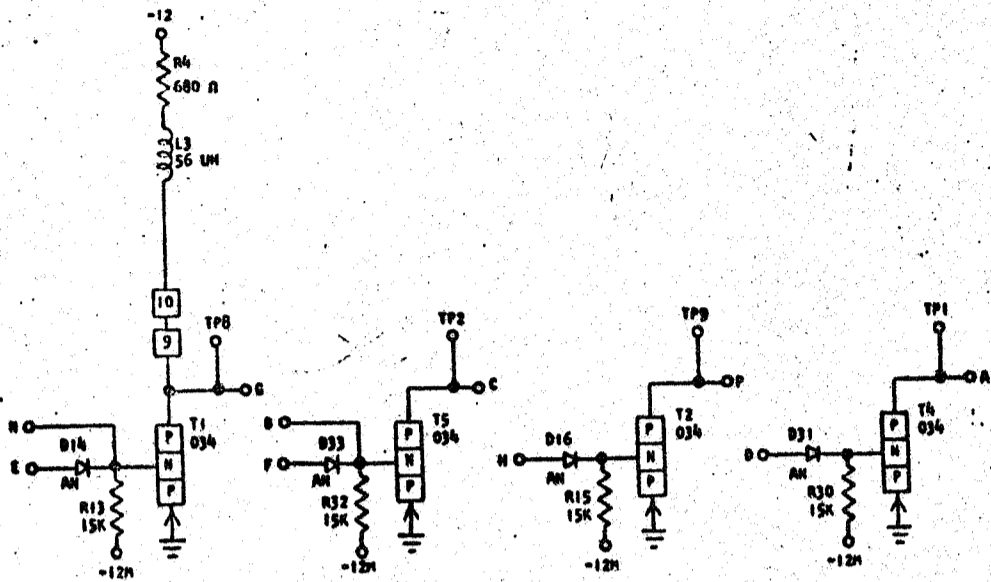
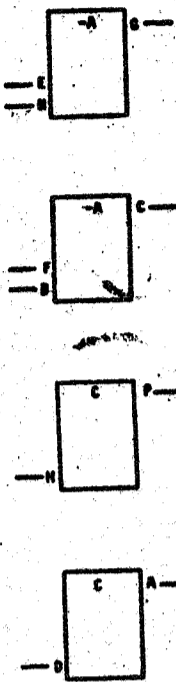


REFERENCE DRAWING
SEE PRODUCTION DRAWING 371278

CTDL - ONE WAY PNP



SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. INPUTS ON EXTENDER CARD MUST BE DOWN IN COINCIDENCE WITH INPUT ON BOARD FOR UP OUTPUT
4. T5, T2, T4, COLLECTORS MUST BE LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

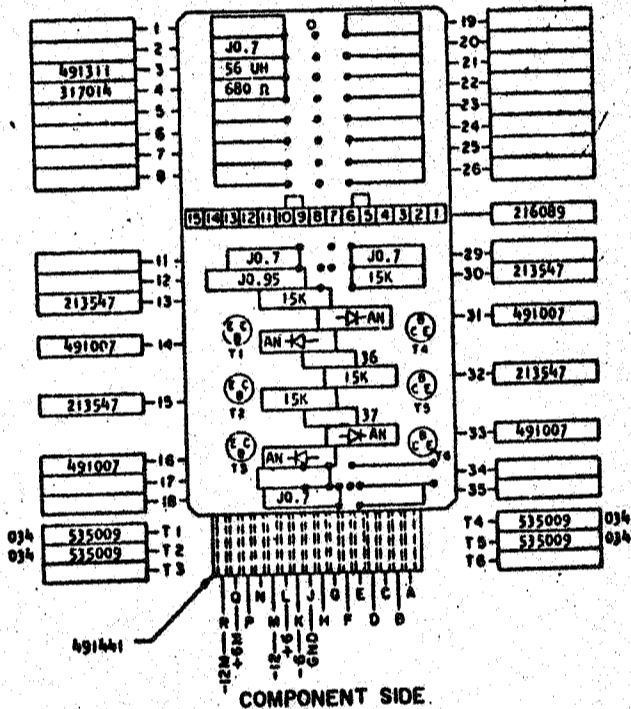
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
E, F, T	INPUT	[Waveform]	UP 1.44	6.24
N, B	EXTENDER INPUT	[Waveform]	DOWN -0.74	-6.24
G, C, U	OUTPUT	[Waveform]	UP +6	
H, D, Y	INPUT	[Waveform]	DOWN 0.0	
P, A, V	OUTPUT	[Waveform]	UP -0.54	0.24
			DOWN -7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF 'OR'.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASH TSTR-CTDL-ONE	DATE	4-29-62	CHANGE NO.	EC115599	APPROVAL		DATE		DEVELOPMENT NO.	729846
NAME	WAY PNP	DATE	30.6.63	CHANGE NO.	JTB3687	APPROVAL		DATE		DEVELOPMENT NO.	
DESIGN	NO	SCALE	3-1-62	SCALE	NONE	APPROVAL		DATE		DEVELOPMENT NO.	
CHECK	MN	DRAW	3-1-62	DRAW	LIG	3-17-62		DATE		DEVELOPMENT NO.	
APPROV		CHECK		CHECK				DATE		DEVELOPMENT NO.	

729846