

729918

STANDARD CODE

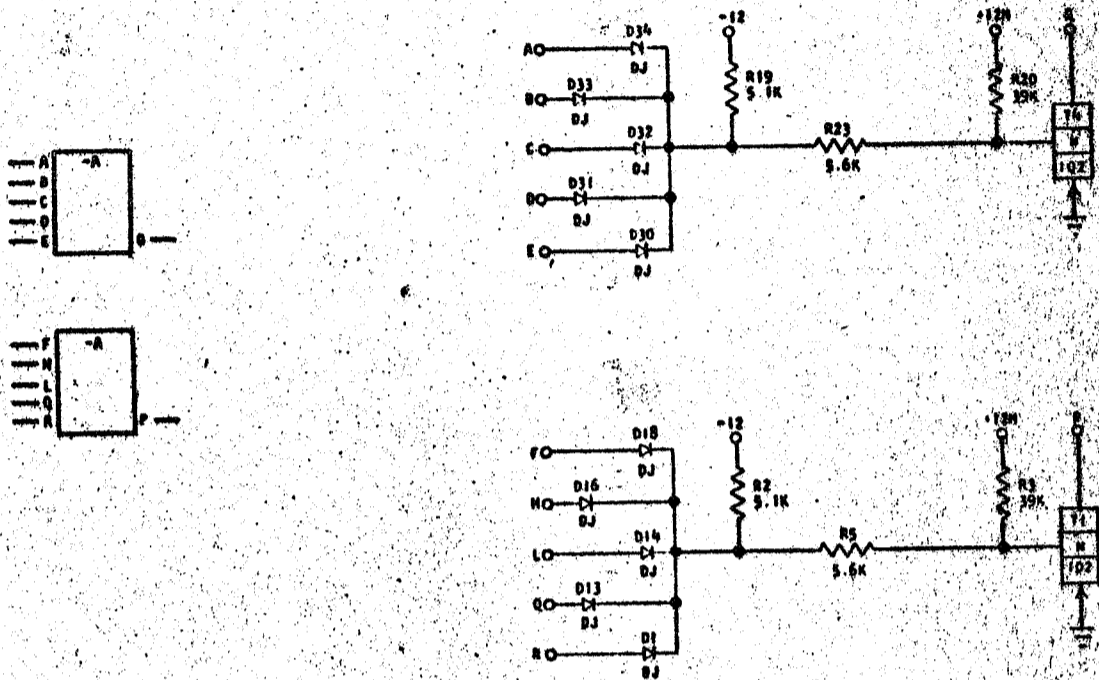
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D.G.Y.

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370375

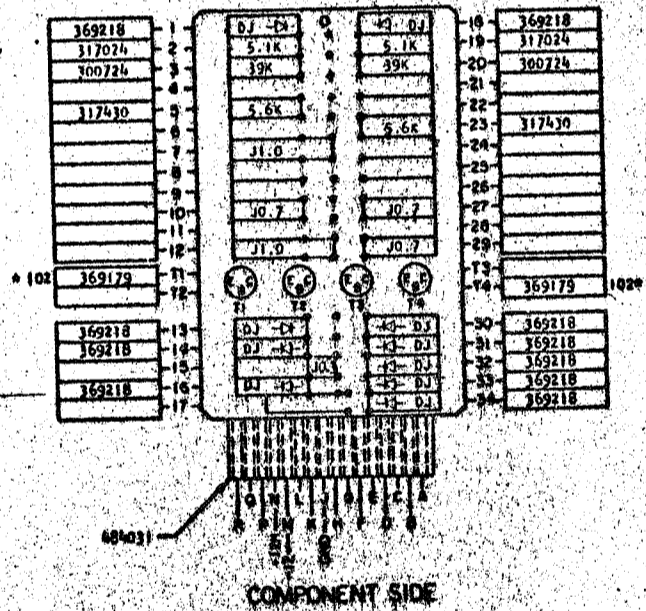
SOTDL 5-WAY LOGIC BLOCK LOW SPEED WITHOUT LOAD



SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
A, F	Y INPUT	[Waveform]	UP	-0.65 - -1
B, H	Y INPUT	[Waveform]	UP	-5.8 - -8.8
C, L	Y INPUT	[Waveform]	UP	-0.65 - -1
D, Q	Y INPUT	[Waveform]	UP	-5.8 - -8.8
E, R	Y INPUT	[Waveform]	UP	-0.65 - -1
G, P	Y OUTPUT	[Waveform]	UP	-5.8 - -8.8



DELAY: SOTDL - LOW SPEED  
 LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

TURN ON (NSEC)	MIN 75	MAX 100
TURN OFF (NSEC)	NO	200

\*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

\*THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SOTDL 5-WAY	4-29-62	RC 115599					729918
LOGIC BLOCK LOW SPEED W/O LOAD	30.0-63 TT 83687						
DESIGN NO	3-1-62	SCALE	ROME				
CHECK NO	3-1-62	DRAW	LIG	3-P68			
APPROV		CHECK					

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