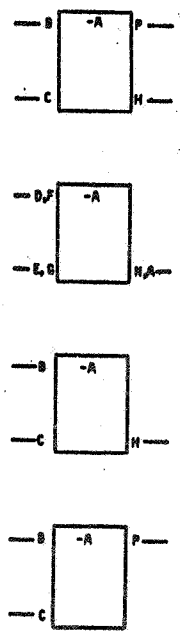
STANDARDS CODE 729869

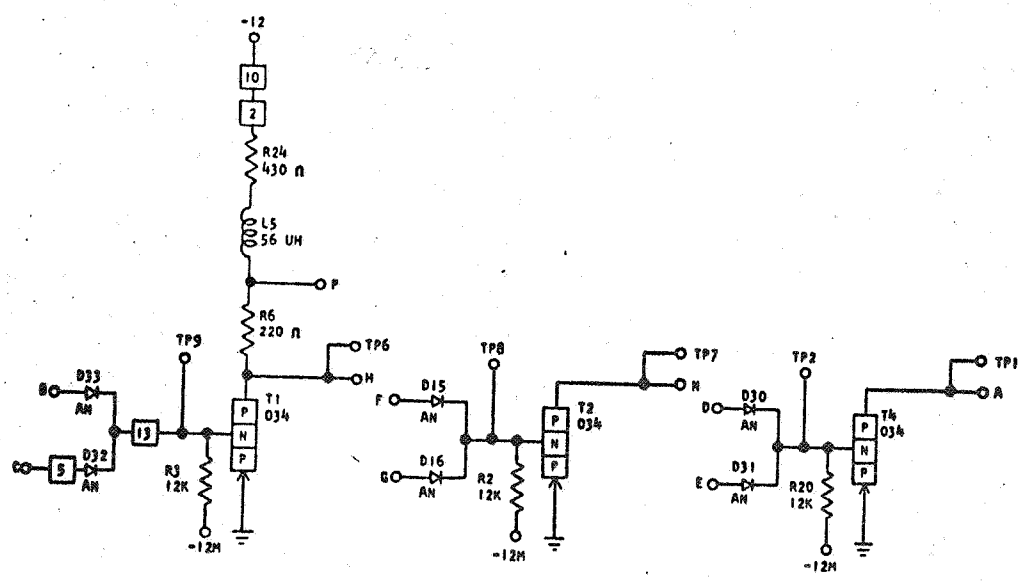
CARD CODE 729869
JG VV

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371582

CTDL HIGH SPEED-TWO WAY "AND" PNP ONE LOAD

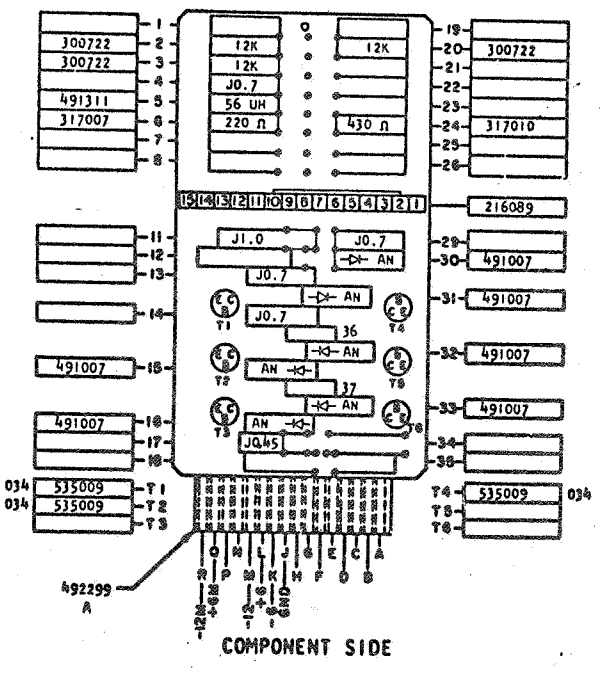




SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON THE OUTPUT IS UP
3. T2, T4 MUST BE COLLECTOR LOADED
4. PIN P IS CURRENT MODE OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
B,C	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
H	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48
P	P	OUTPUT		UP	-4.93	-3.54
				DOWN	-8.82	-12.48
D,F, E,G	T	INPUT		UP	+1.44	+6.24
				DOWN	-.74	-6.24
N,A	U	OUTPUT		UP	-.54	+.24
				DOWN	-7.44	-12.48



DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS.
EXAMPLE: LOGIC BLOCK DRIVING EF "OR".

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR- CTDL HIGH SPEED-TWO WAY "AND" PNP ONE LOAD					6-29-62	EC115599					729869
DESIGN			MODEL	SMS		30-4-63	7783687					
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG	3-17-62							
APPRO			CHECK									

C