

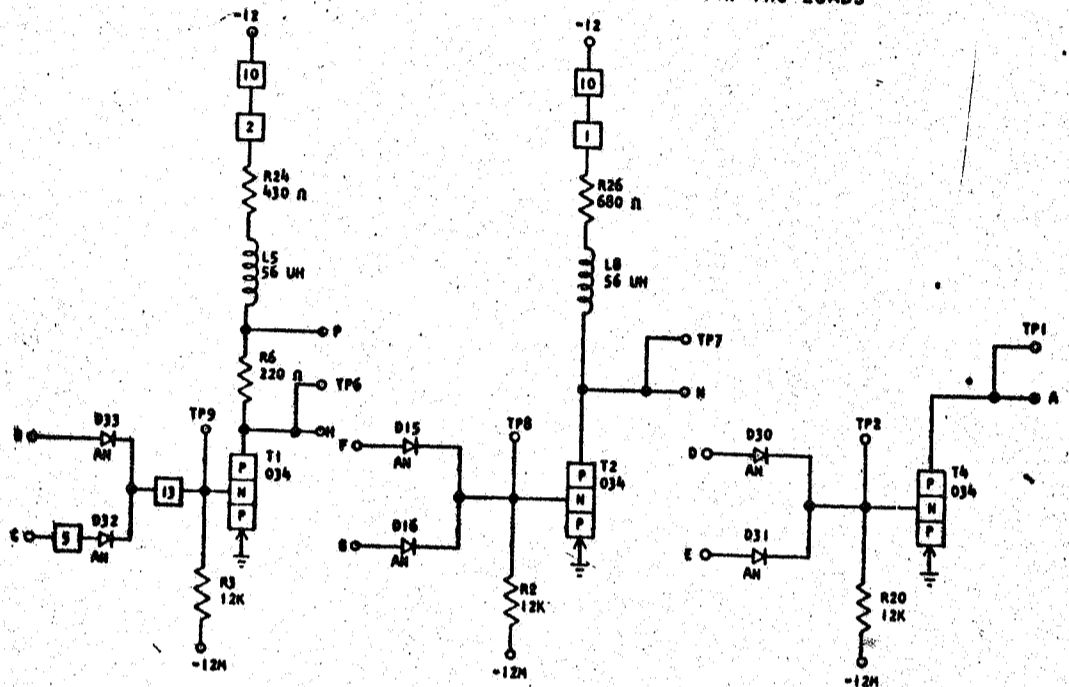
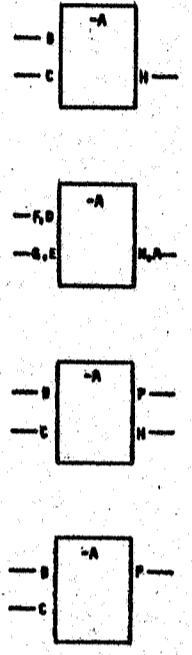
729870

STANDARD
FORM

CARD CODE 729870
JG VW

REFERENCE DRAWING
SEE PRODUCTION DRAWING 371581

CTDL HIGH SPEED - TWO WAY "AND" PNP TWO LOADS



SEQUENCE OF OPERATION

1. ANY INPUT UP, THE TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. T4 MUST BE COLLECTOR LOADED
4. PIN P IS CURRENT MODE OUTPUT
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

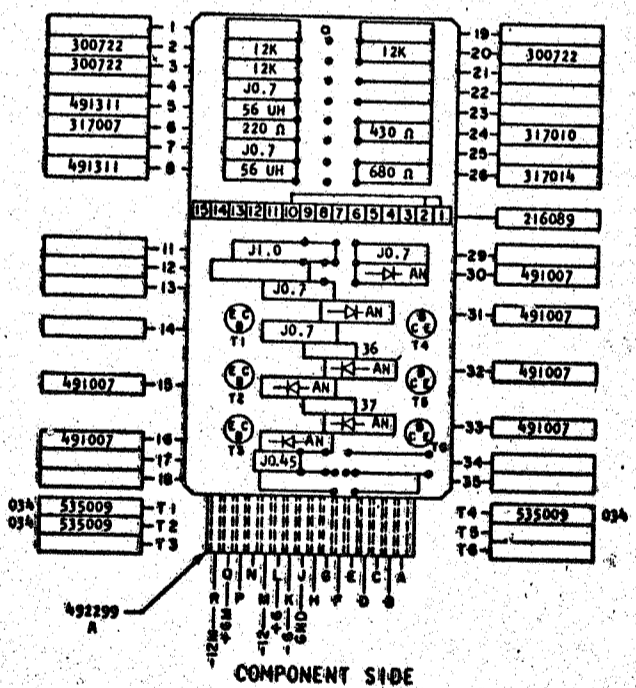
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
B, C	T	INPUT	UP +4.44	+6.24
			DOWN -7.4	-6.24
N	U	OUTPUT	UP -5.4	+2.4
			DOWN -7.44	-12.48
P	P	OUTPUT	UP -4.93	-3.54
			DOWN -8.82	-12.48
F, G	T	INPUT	UP +4.44	+6.24
			DOWN -7.4	-6.24
N	U	OUTPUT	UP -5.4	+2.4
			DOWN -7.44	-12.48
B, C	T	INPUT	UP +1.44	+6.24
			DOWN -7.4	-6.24
A	U	OUTPUT	UP -5.4	+2.4
			DOWN -7.44	-12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*TIMES DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING BY 'ON'.



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.		DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH	6-27-62	EC 115599					
SPEED-TWO WAY "AND" PNP TWO LOADS								
DESIGN								
DETAIL	RQ 3-1-62	SCALE	NONE					
CHECK	MM 3-1-62	DRAW	LIG 3-1-62					
APPROVAL		CHECK						

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