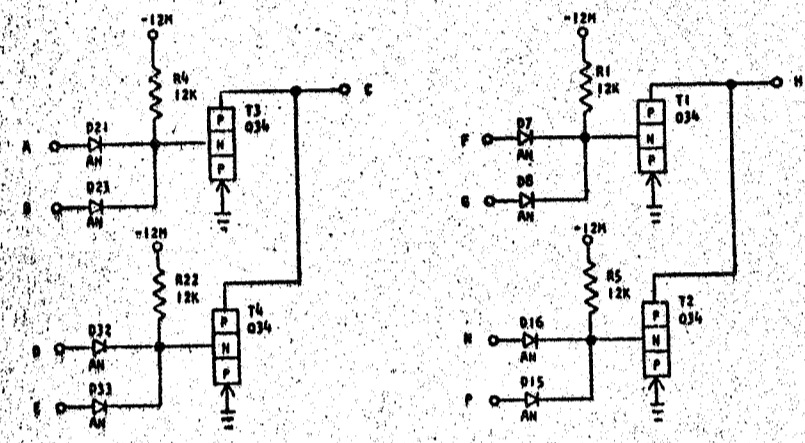
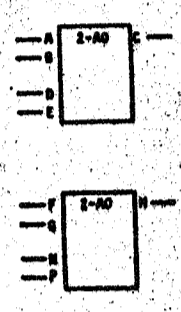


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CARD CODE 729899  
3J MX

REFERENCE DRAWING  
SEE PRODUCTION DRAWING 370J41

CTDL PNP TWO WAY GATE WITHOUT COLLECTOR LOAD



SEQUENCE OF OPERATION

1. BOTH INPUTS TO A TRANSISTOR DOWN, TRANSISTOR ON OUTPUT UP
2. FOR DOWN OUTPUT, EITHER INPUT TO BOTH TRANSISTORS MUST BE UP
3. EXTERNAL LOADING OF COLLECTORS REQUIRED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

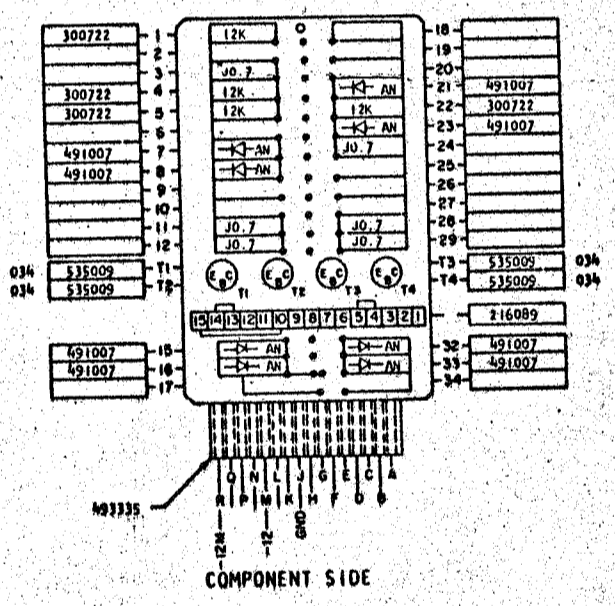
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
A, B, F, G	T	INPUT	UP	1.44 6.24
			DOWN	-0.74 -6.24
H, C, E, P	T	INPUT	UP	1.44 6.24
			DOWN	-0.74 -6.24
C, H	U	OUTPUT	UP	-0.54 0.24
			DOWN	-7.44 -12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.80
TURN OFF	0.05	0.80

\*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASH TSTR-CTDL PNP TWO WAY GATE WITHOUT COLLECTOR LOAD	4-2-62	EC 115599					729899
DESIGN		304-63	5783687				
DESIGNER	3-1-62	SCHE	NONE				
CHECKER	3-1-62	DRAN	LEB 3-17-62				
APPROVER							

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