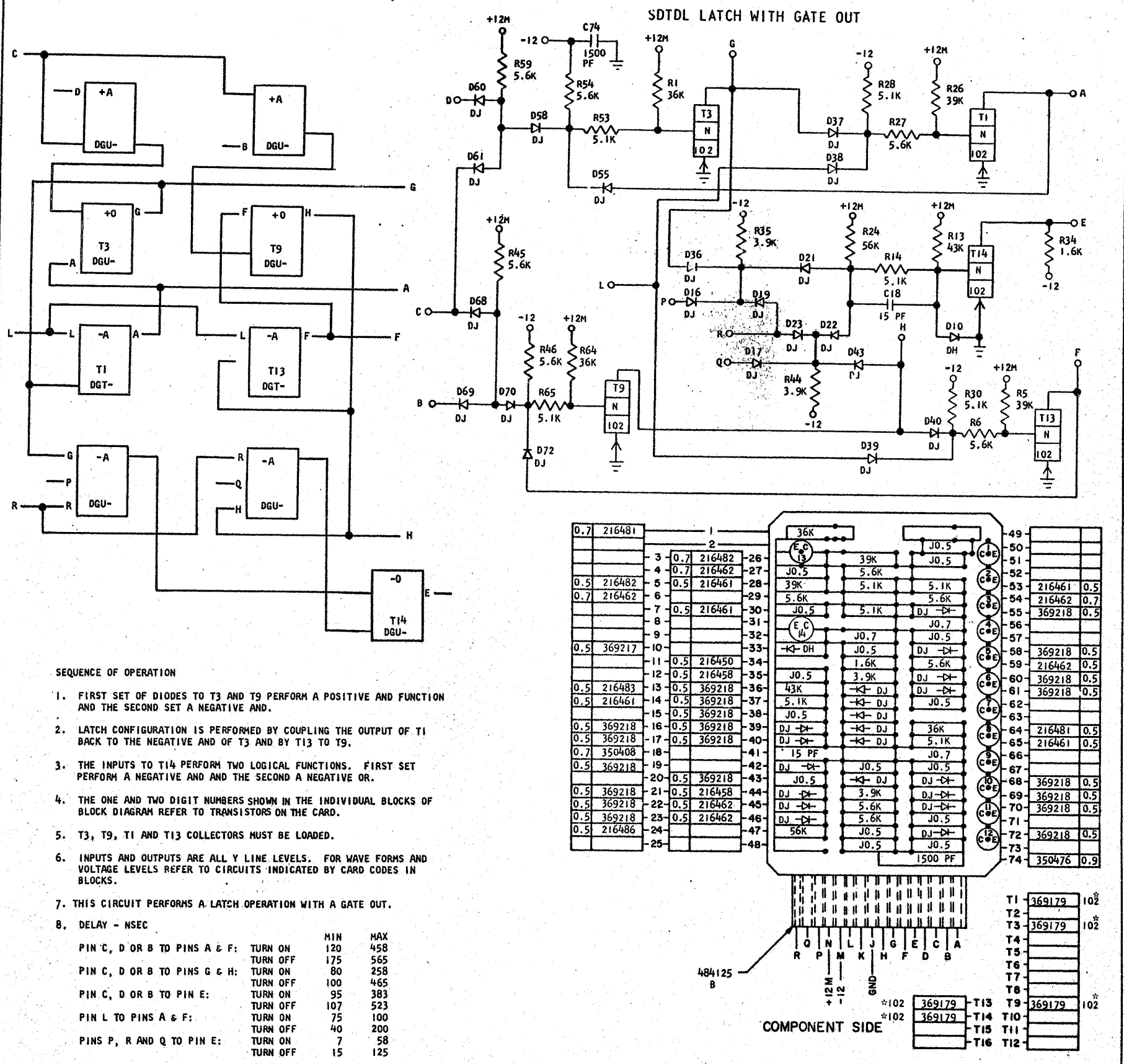
729929 | STANDARDS CODE

CARD CODE 729929
DHK-

REFERENCE DRAWING

SEE PRODUCTION DRAWING 370349



SEQUENCE OF OPERATION

1. FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF TI BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T9.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T9, TI AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN C, D OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN C, D OR B TO PINS G & H:	TURN ON	80	258
	TURN OFF	100	465
PIN C, D OR B TO PIN E:	TURN ON	95	383
	TURN OFF	107	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	40	200
PINS P, R AND Q TO PIN E:	TURN ON	7	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-SDTDL LATCH WITH GATE OUT				2-27-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

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REFERENCE DRAWING

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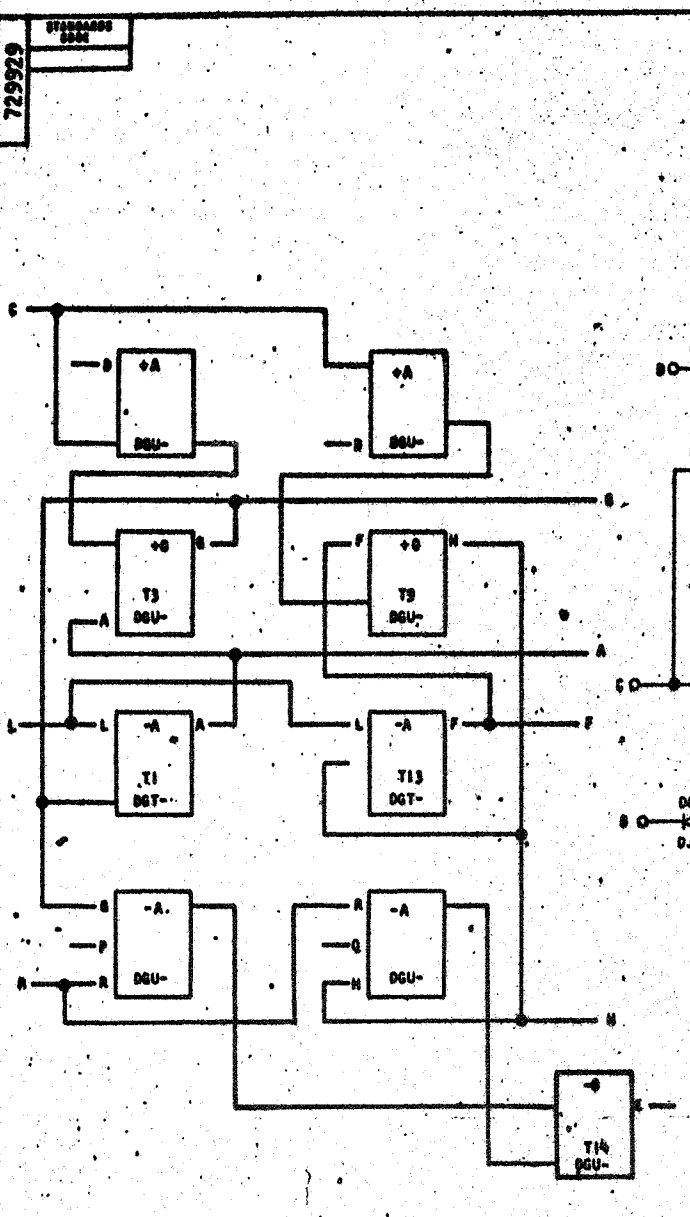
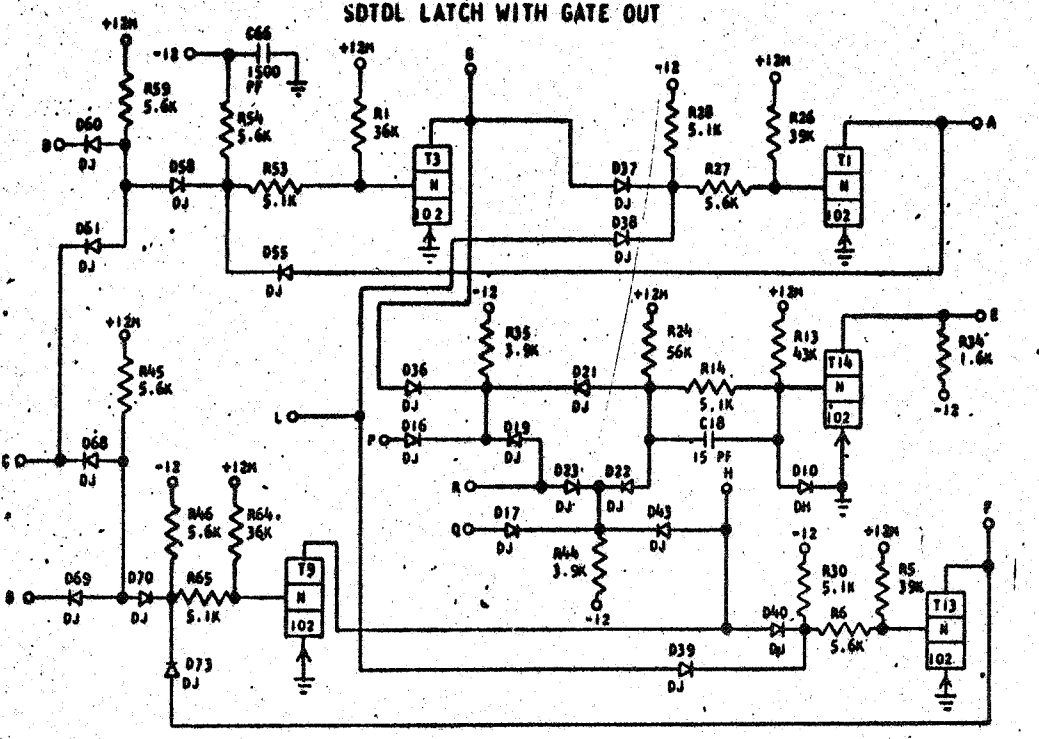
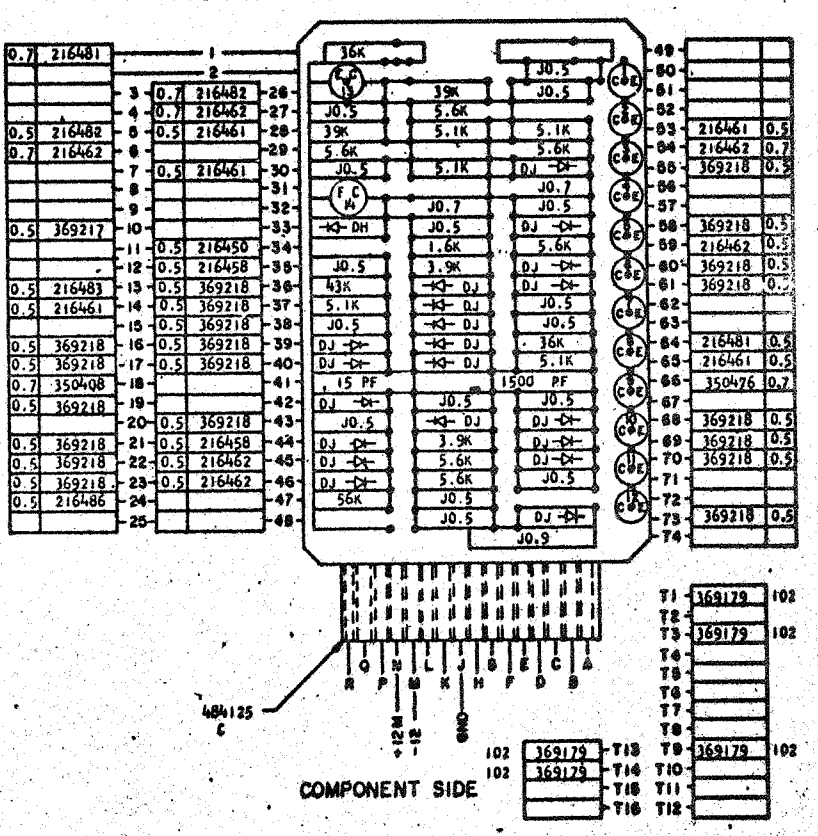
SDTDL LATCH WITH GATE OUT







SEQUENCE OF OPERATION

1. FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T9.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T9, T1 AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN C, B OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN C, B OR B TO PINS G & H:	TURN ON	80	258
	TURN OFF	100	465
PIN C, B OR B TO PIN E:	TURN ON	95	383
	TURN OFF	107	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	40	200
PINS P, R AND Q TO PIN E:	TURN ON	7	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	729929
NAME	CARD ASM TSTR-SDTDL LATCH WITH GATE OUT					2-19-62	115599						
				MODEL	SMS	1-3-63	EC 116034						
DESIGN				SCALE	NONE	30-4-63	JT 83687						
DETAIL	RQ	3-1-62		DRAW	LIG 3-17-62								
CHECK	WH	3-1-62		CHECK									
APPRD													

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CARD CODE 729929

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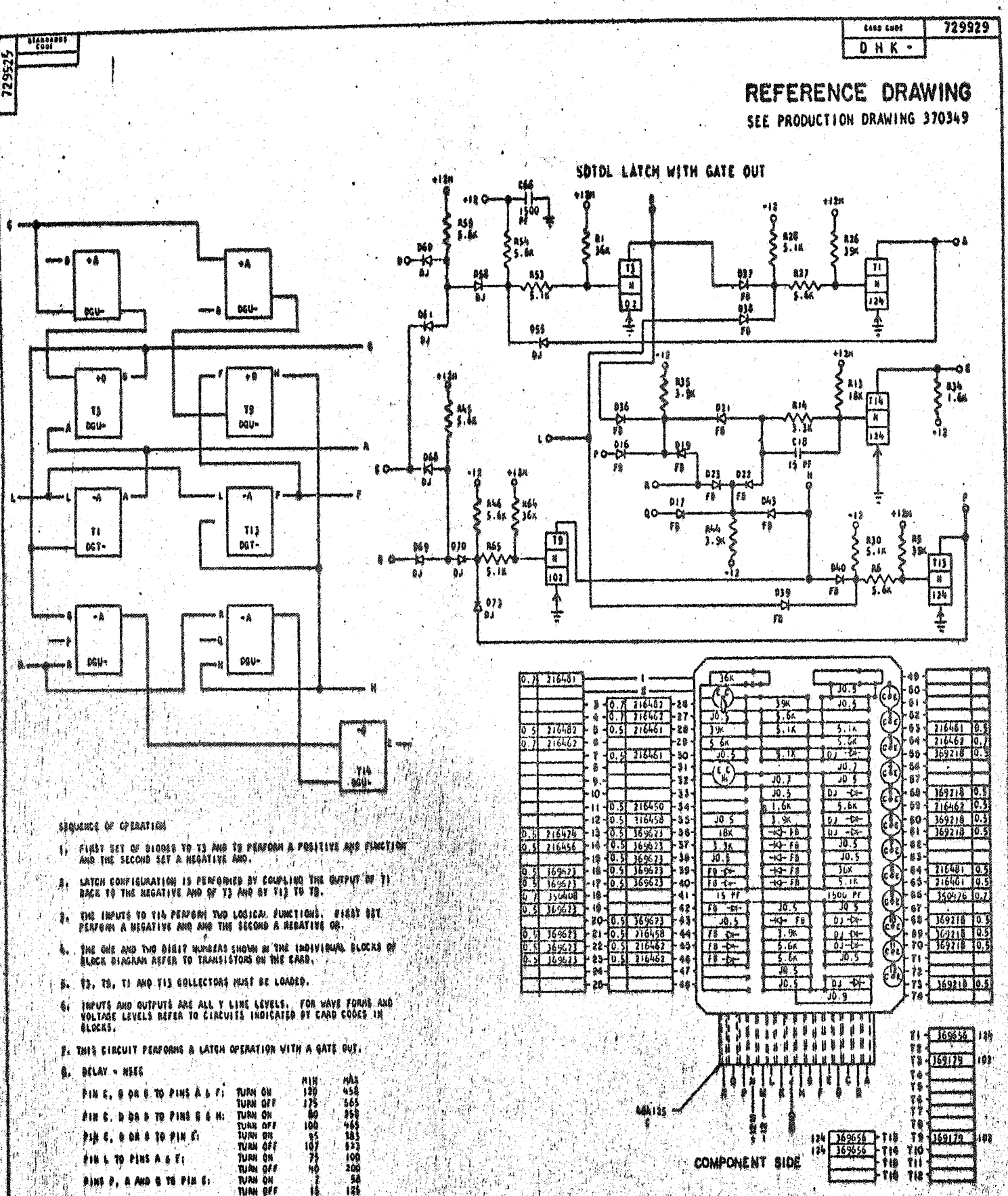
REFERENCE DRAWING

SEE PRODUCTION DRAWING 370349



SEQUENCE OF OPERATION

1. FIRST SET OF BLOCKS TO T3 AND T8 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
2. LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T8.
3. THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
4. THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
5. T3, T8, T1 AND T13 COLLECTORS MUST BE LOADED.
6. INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORM AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
7. THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
8. DELAY - NSEC

		MIN	MAX
PIN E, B OR B TO PINS A & F:	TURN ON	120	458
	TURN OFF	175	565
PIN G, B OR B TO PINS G & H:	TURN ON	80	358
	TURN OFF	100	465
PIN G, B OR B TO PIN F:	TURN ON	95	183
	TURN OFF	167	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	90	200
PINS P, R AND Q TO PIN G:	TURN ON	2	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVED	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME KAMS ASM TSTG-SDTDL LATCH WITH GATE OUT	7-19-62	115599					
	8-3-63	116034					
DESIGN RG 7-1-62	8-10-63	116186					
CHECK WS 7-1-62							
APPD							

729929

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