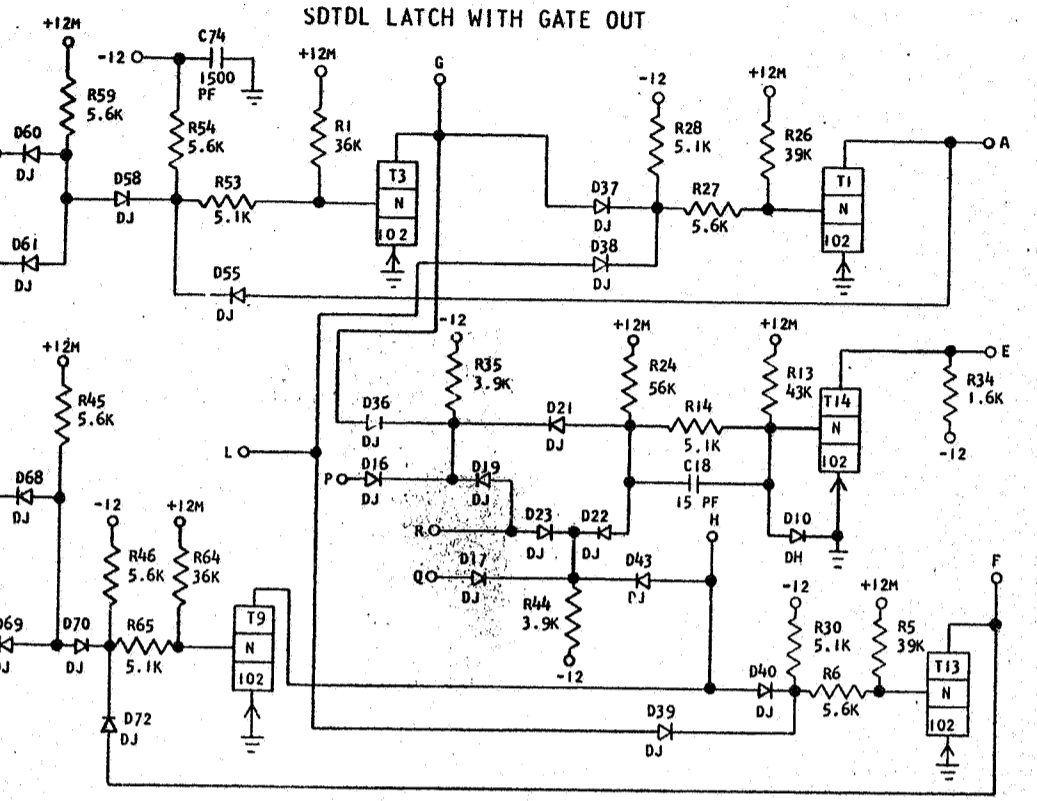
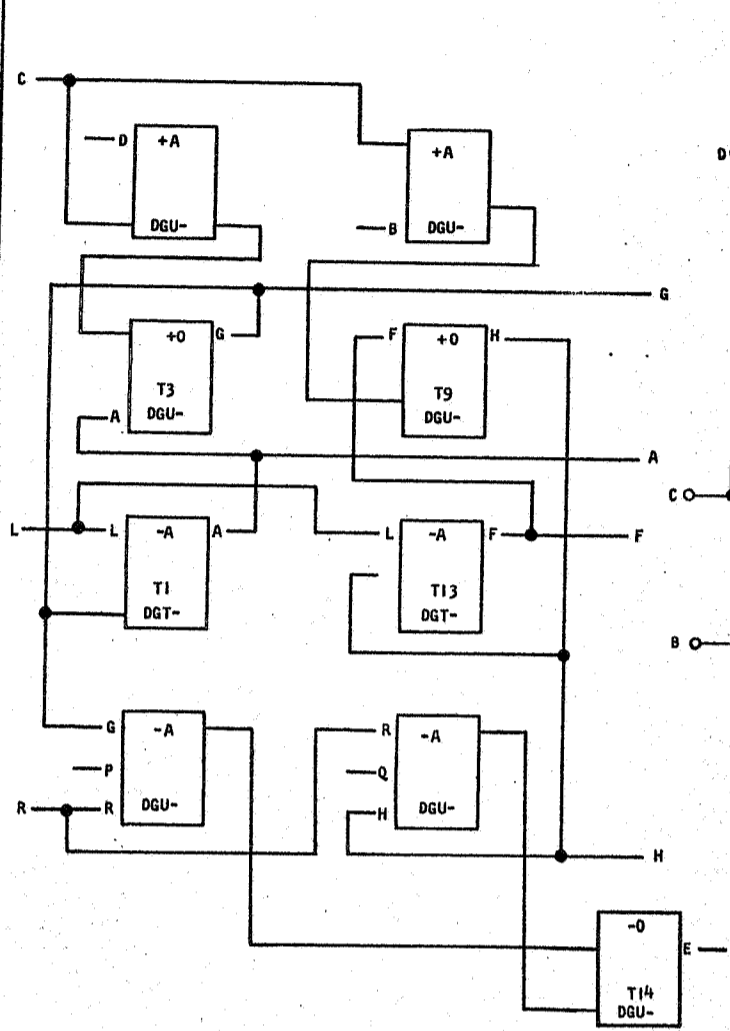


STANDARDS CODE
729929

CARD CODE 729929
D H K -

REFERENCE DRAWING
SEE PRODUCTION DRAWING 370349



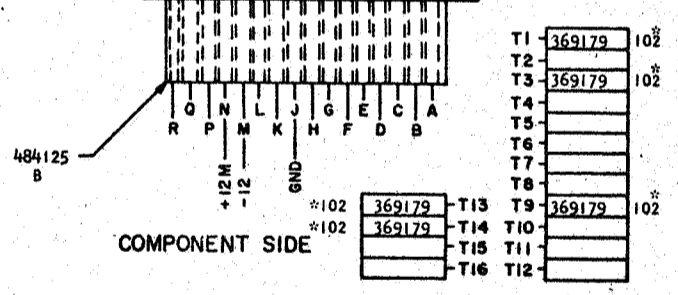
SEQUENCE OF OPERATION

- FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
- LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T3 TO T9.
- THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
- THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
- T3, T9, T1 AND T13 COLLECTORS MUST BE LOADED.
- INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
- THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
- DELAY - NSEC

PIN C, D OR B TO PINS A & F:	TURN ON	MIN	MAX
	TURN ON	120	458
	TURN OFF	175	565
PIN C, D OR B TO PINS G & H:	TURN ON	80	258
	TURN OFF	100	465
PIN C, D OR B TO PIN E:	TURN ON	95	383
	TURN OFF	107	523
PIN L TO PINS A & F:	TURN ON	75	100
	TURN OFF	40	200
PINS P, R AND Q TO PIN E:	TURN ON	7	58
	TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.

0.7	216481	1	36K	49	
3	0.7 216482	26		50	
4	0.7 216462	27		51	
5	0.5 216482	28		52	
6	0.5 216461	29		53	216461 0.5
7	0.7 216462	30		54	216462 0.7
8		31		55	369218 0.5
9		32		56	
10	0.5 369217	33		57	
11		34		58	369218 0.5
12	0.5 216450	35		59	216462 0.5
13	0.5 216483	36		60	369218 0.5
14	0.5 216461	37		61	369218 0.5
15	0.5 369218	38		62	
16	0.5 369218	39		63	
17	0.5 369218	40		64	216481 0.5
18	0.7 350408	41		65	216461 0.5
19	0.5 369218	42		66	
20	0.5 369218	43		67	
21	0.5 369218	44		68	369218 0.5
22	0.5 369218	45		69	369218 0.5
23	0.5 369218	46		70	369218 0.5
24	0.5 216486	47		71	
		48		72	369218 0.5
				73	
				74	350476 0.9



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SDTD LATCH WITH GATE OUT				7-62	115599					729929
DESIGN	RQ	3-1-62	MODEL	SMC						
DETAIL	WH	3-1-62	SCALE	NONE						
CHECK	WH	3-1-62	DRAW	LIG	3-17-62					
APPRO			CHECK							

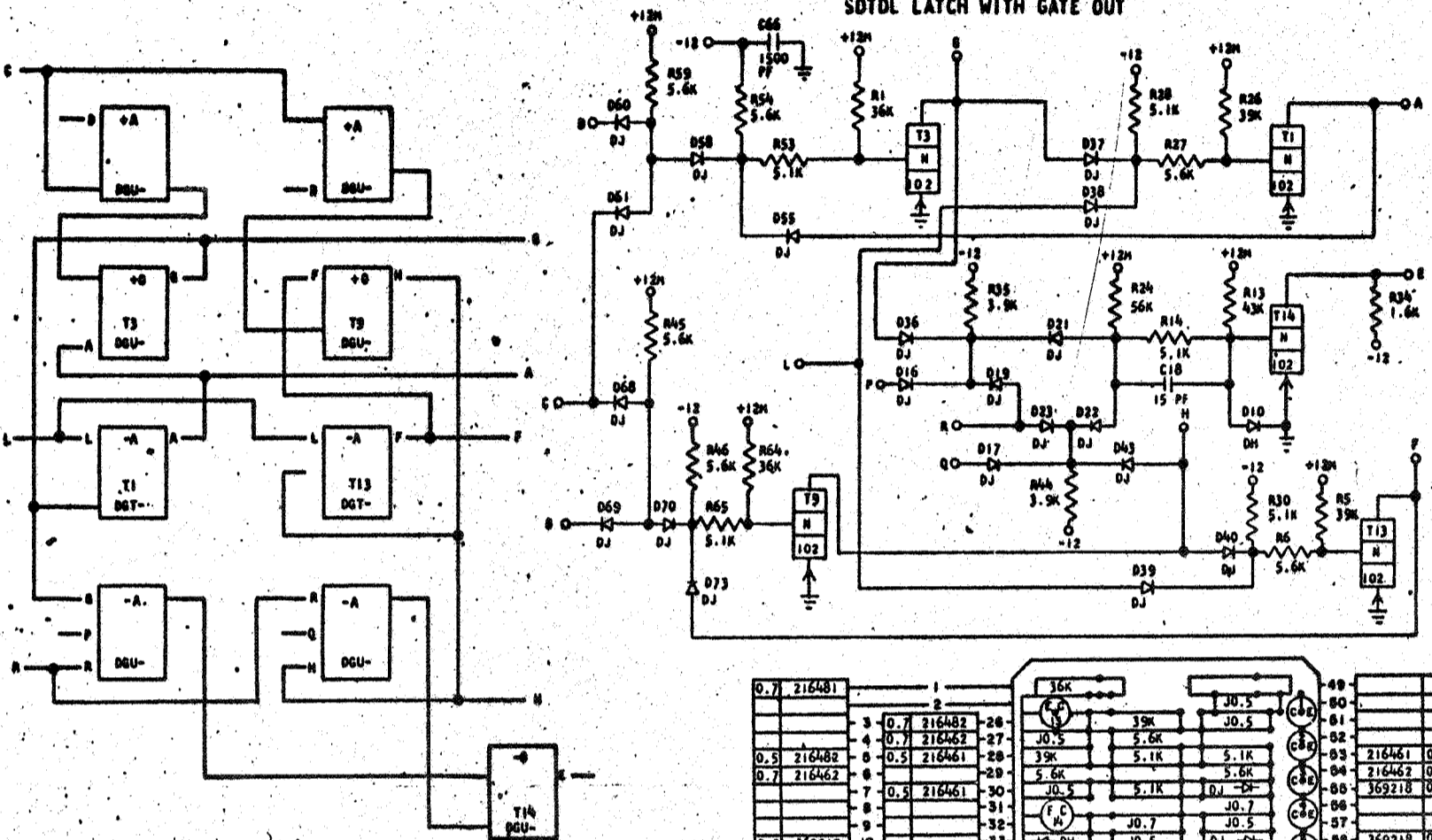
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STANDARD
DRAWING

729929
D H K -

REFERENCE DRAWING SEE PRODUCTION DRAWING 370349

SOTDL LATCH WITH GATE OUT



SEQUENCE OF OPERATION

- FIRST SET OF DIODES TO T3 AND T9 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
- LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND OF T3 AND BY T13 TO T9.
- THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
- THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
- T3, T9, T1 AND T13 COLLECTORS MUST BE LOADED.
- INPUTS AND OUTPUTS ARE ALL V LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.
- THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.
- DELAY - NSEC

PIN C, D OR B TO PINS A & F:	MIN	MAX
TURN ON	120	458
TURN OFF	175	565

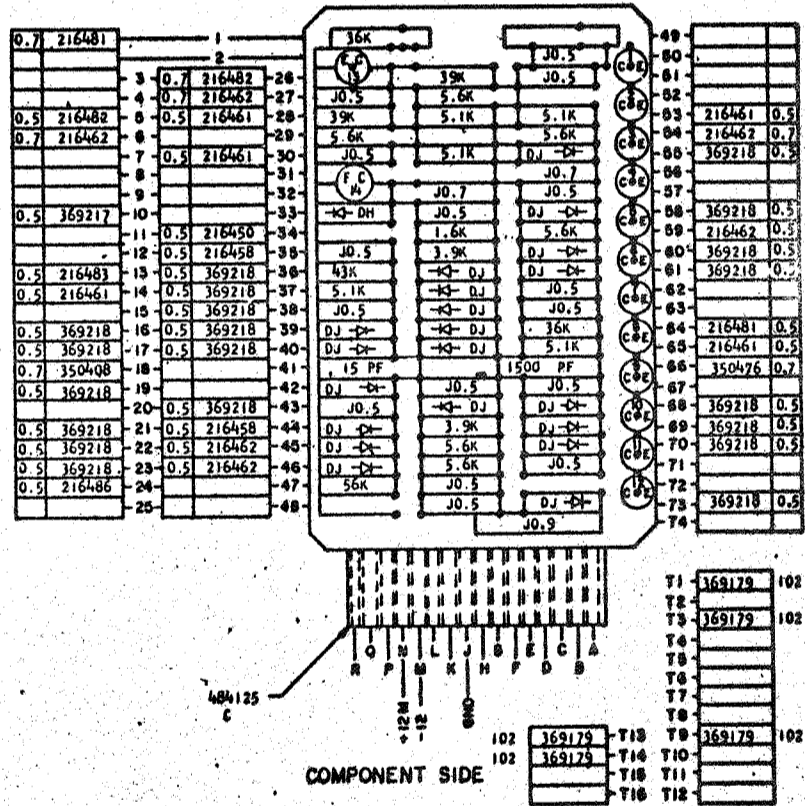
PIN C, D OR B TO PINS G & H:	MIN	MAX
TURN ON	80	258
TURN OFF	100	465

PIN C, D OR B TO PIN E:	MIN	MAX
TURN ON	95	383
TURN OFF	107	523

PIN L TO PINS A & F:	MIN	MAX
TURN ON	75	100
TURN OFF	40	200

PINS P, R AND Q TO PIN E:	MIN	MAX
TURN ON	7	58
TURN OFF	15	125

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

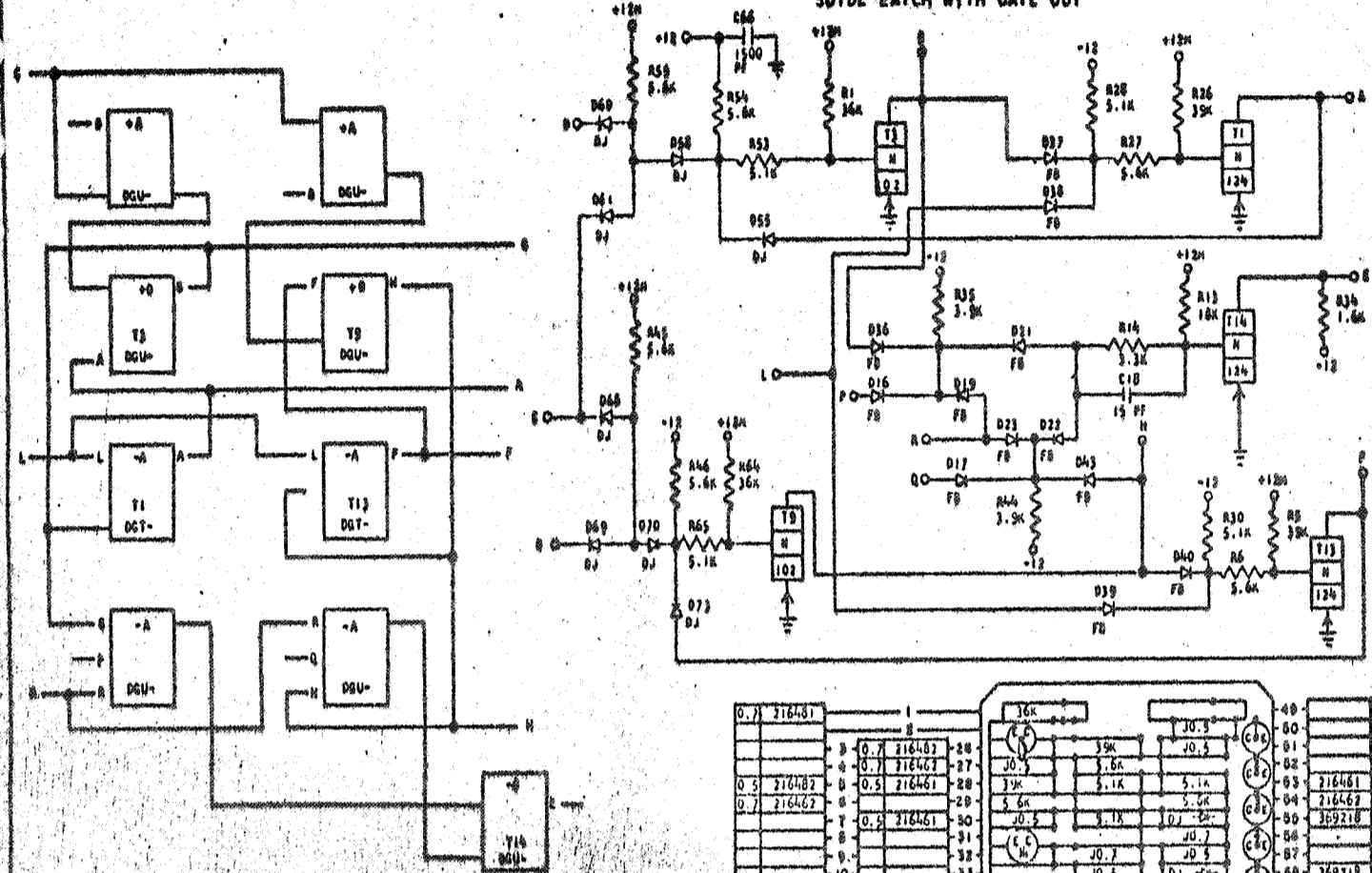
INTERNATIONAL BUSINESS MACHINES CORP.		DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME CARD ASM TSTR-SOTDL LATCH		1-17-62	115599					729929
WITH GATE OUT		1-3-63	EC 116034					
DESIGN	RD	3-1-62	SCALE	SMS	30-4-63	JT 83687		
DETAIL	WH	3-1-62	DRAW	NOML				
CHECK			LIG	13-17-62				
APPROV			CHECK					

729929

CARD CODE
D H K - 729929

REFERENCE DRAWING SEE PRODUCTION DRAWING 370349

SOTDL LATCH WITH GATE OUT



SEQUENCE OF OPERATION

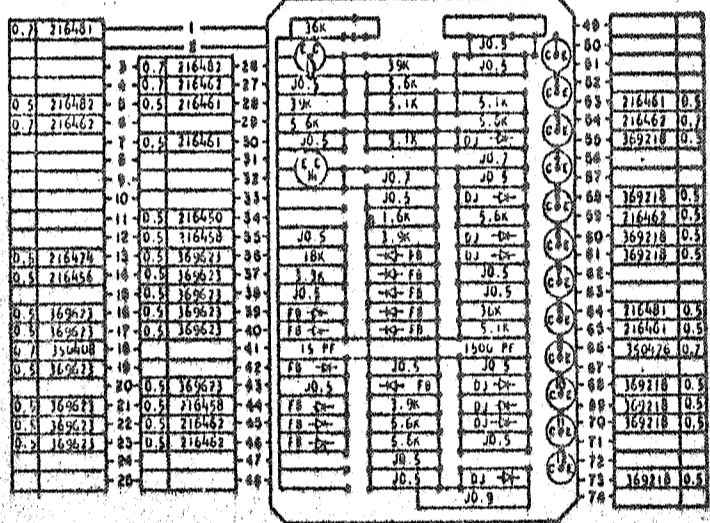
- FIRST SET OF DIODES TO T3 AND T5 PERFORM A POSITIVE AND FUNCTION AND THE SECOND SET A NEGATIVE AND.
- LATCH CONFIGURATION IS PERFORMED BY COUPLING THE OUTPUT OF T1 BACK TO THE NEGATIVE AND BY T3 AND BY T13 TO T8.
- THE INPUTS TO T14 PERFORM TWO LOGICAL FUNCTIONS. FIRST SET PERFORM A NEGATIVE AND AND THE SECOND A NEGATIVE OR.
- THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.
- T3, T8, T1 AND T13 COLLECTORS MUST BE LOADED.
- INPUTS AND OUTPUTS ARE ALL Y LINE LEVELS. FOR WAVE FORMS AND VOLTAGE LEVELS REFER TO CIRCUITS INDICATED BY CARD CODES IN BLOCKS.

THIS CIRCUIT PERFORMS A LATCH OPERATION WITH A GATE OUT.

DELAY - NSEC

TRANSISTOR	MIN	MAX
PIN C, D OR E TO PINS A & F:		
TURN ON	130	450
TURN OFF	175	565
PIN C, D OR E TO PINS G & H:		
TURN ON	80	250
TURN OFF	100	465
PIN C, D OR E TO PIN I:		
TURN ON	85	285
TURN OFF	105	355
PIN L TO PINS A & F:		
TURN ON	75	100
TURN OFF	90	200
PINS P, R AND S TO PIN G:		
TURN ON	7	50
TURN OFF	10	120

NOTE: THESE DELAYS BASED ON A .68K LOAD RESISTOR AT PINS G AND H AND A .56K LOAD RESISTOR AT PINS A AND F. THEY CAN BE EXCEEDED WITH A LARGER COLLECTOR RESISTOR.



COMPONENT SIDE

APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.	DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
REVISION 100	1-1-62	118999					729929
REVISION 101	1-1-62	119000					
REVISION 102	4-10-62	119100					

729929