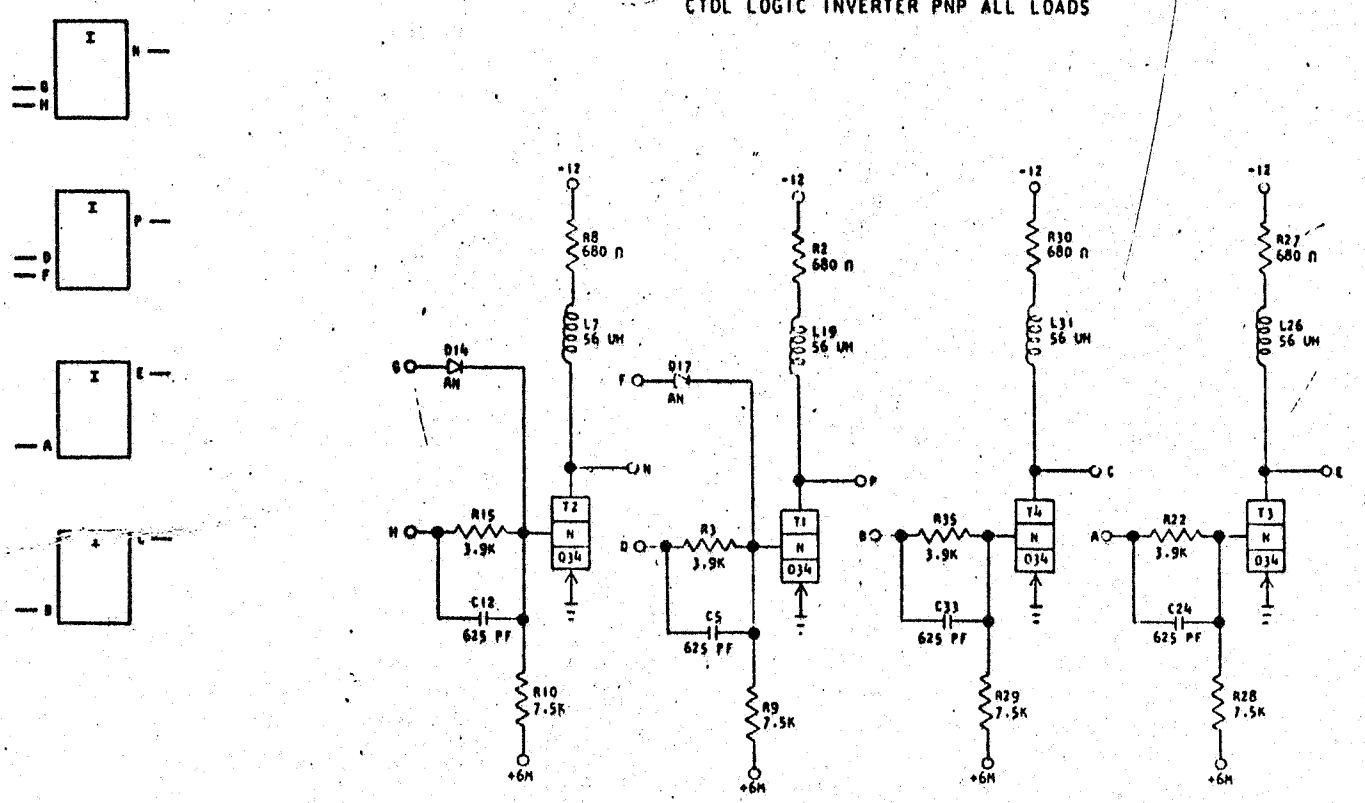
729879 STANDARDS COPY

CARD CODE	729879
JL VB	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371077

CTDL LOGIC INVERTER PNP ALL LOADS



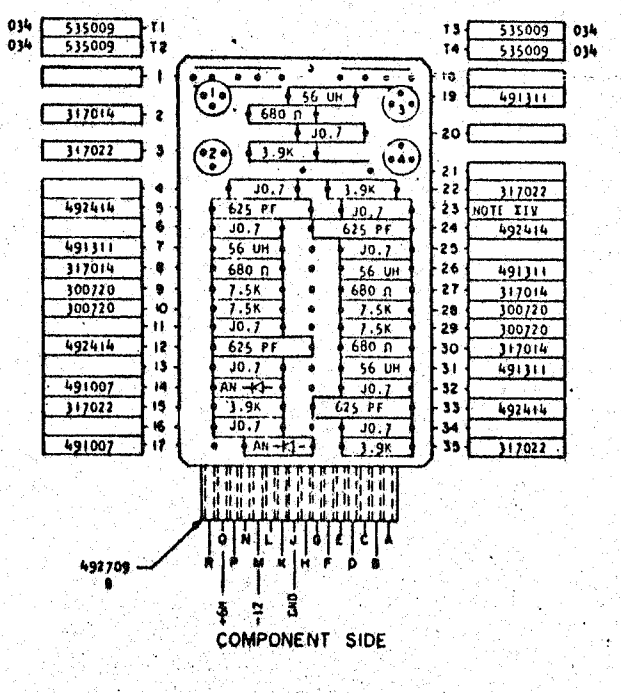
SEQUENCE OF OPERATION

1. FOR AN UP OUTPUT THE INPUT MUST BE DOWN
2. THE GATING DIODE IS PROVIDED ONLY TO RESET A LOGIC INVERTER LATCH. IT SHOULD NOT BE USED AS A SIGNAL INPUT SINCE IT IS POSSIBLE FOR THE SIGNAL INPUT TO OVERRIDE THE GATE
3. IN APPLICATIONS USING BOTH INPUTS ON CIRCUITS 1 AND 2 THE GATE (PINS G OR F) AND SIGNAL INPUTS MUST BE DOWN FOR AN UP OUTPUT
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
H,D	U	INPUT SIGNAL		UP	-0.54	+0.24
				DOWN	-7.44	-12.48
G,F	T	INPUT GATE		UP	+1.44	+6.24
				DOWN	-0.74	-6.24
H,P	U	OUTPUT		UP	-0.54	+0.24
				DOWN	-7.44	-12.48
A,B, H,D	U	INPUT		UP	0.54	+0.24
				DOWN	-7.44	-12.48
E,C, P,N	U	OUTPUT		UP	-0.54	+0.24
				DOWN	-7.44	-12.48

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	-0.05	-0.15
TURN OFF	+0.05	+0.55



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.	
NAME	CARD ASM TSTR - CTDL LOGIC INVERTER PNP ALL LOADS				6-29-62	EC 115599						729879
					30.4.63	TT83687						
DESIGN			MODEL	SMS								
DRAWN	RQ	3-1-62	SCALE	NONE								
CHECK	WH	3-1-62	DRAW	LIG 3-17-62								
APPRD			CHECK									

C

729879