STANDARDS CODE 729844

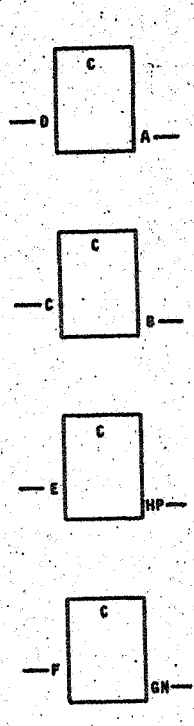
CARD CODE 729844

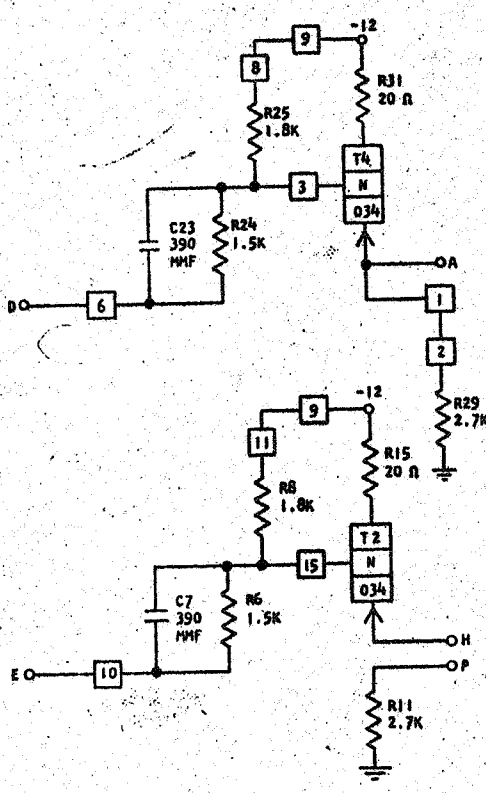
CP WU

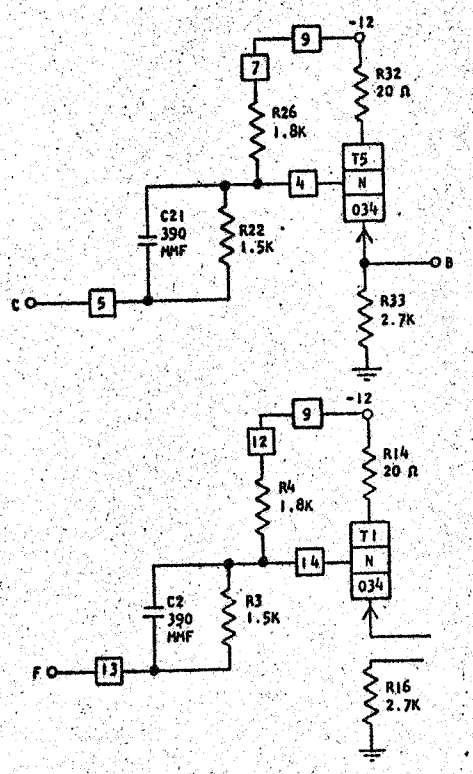
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371257

CTDL - TRANSLATE BLOCK - PNP







SEQUENCE OF OPERATION

1. OUTPUT WILL FOLLOW INPUT, TRANSISTOR ALWAYS IN CONDUCTION
2. LOGICAL FUNCTIONS PREFORMED WHEN OUTPUTS SHARE COMMON LOAD
3. T1, T2 EMITTER MUST BE LOADED

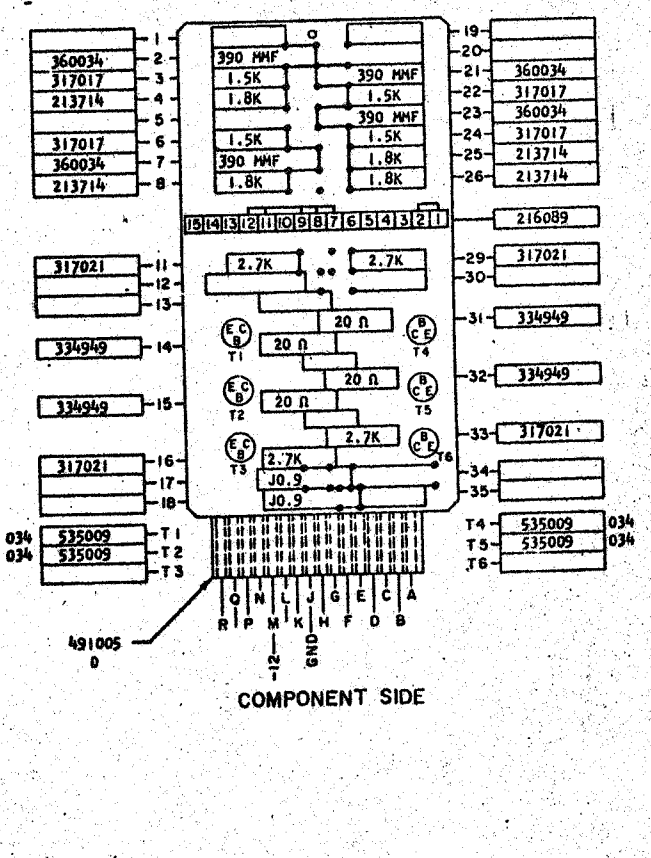
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
D,C E,F	T	INPUT		UP	1.44	6.24
				DOWN	-5.5	-6.24
A,B H,G	U	OUTPUT		UP	-5.2	-0.8
				DOWN	-7.4	-9.2

DELAY

THE DELAY CHARACTERISTICS OF THE TRANSLATE BLOCK ARE SIMILAR TO THOSE OF THE EF.

NO APPRECIABLE DELAY SHOULD BE NOTICED WHEN THE DRIVING BLOCK IS TURNED ON OR OFF.

APPRECIABLE DELAY CAN BE OBSERVED (1 TO 2.5 USEC.) WHEN THE DRIVING BLOCK IS TURNED ON AND THE OUTPUT OF THE TRANSLATE BLOCK IS DRIVING SIGNIFICANT WIRING CAPACITANCE (SEVERAL FEET OF WIRE FROM ONE GATE TO ANOTHER).



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR -CTDL TRANSLATE BLOCK - PNP					4 -62	115599					729844
DESIGN			MODEL	SMS								
DETAIL	RQ	3-1-62	SCALE	NONE								
CHECK	WM	3-1-62	DRAW	LJG	3-17-62							
APPRO			CHECK									

729844

C