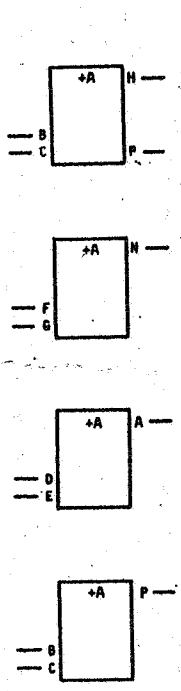
STANDARDS CODE
729825

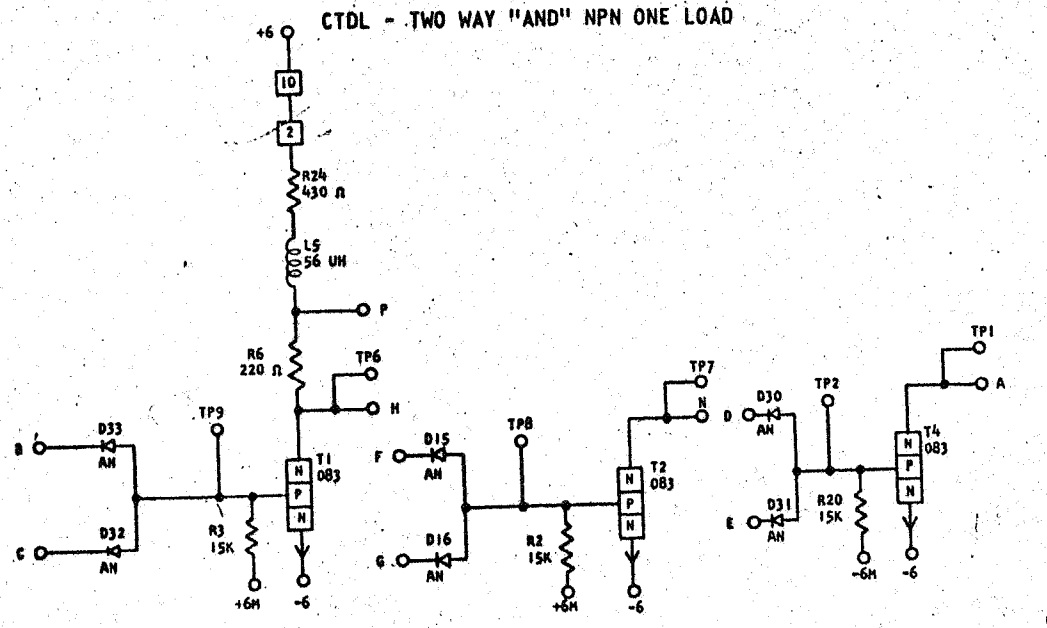
CARD CODE	729825
CH VV	

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371265



CTDL - TWO WAY "AND" NPN ONE LOAD



SEQUENCE OF OPERATION

1. BOTH INPUTS UP, TRANSISTOR ON, OUTPUT DOWN
2. ANY INPUT DOWN, TRANSISTOR OFF, OUTPUT UP
3. T2, T4 COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

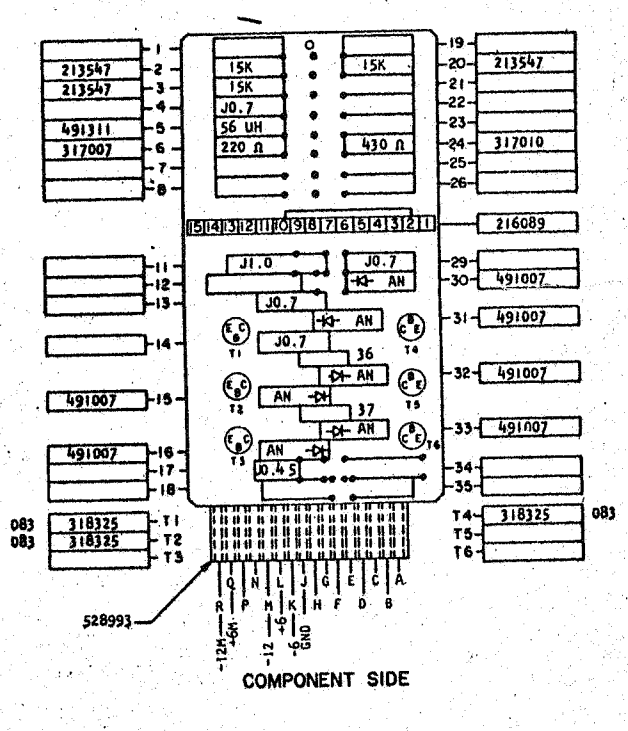
PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
B,F,D	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
C,G,E	U	INPUT		UP	-5.26	0.24
				DOWN	-7.44	-12.5
H,N,A	T	OUTPUT		UP	1.44	6.24
				DOWN	-5.46	-6.24
P	N	OUTPUT		UP	2.82	6.24
				DOWN	-1.07	-2.40

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.05	0.70
TURN OFF	0.05	1.50*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS.
EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL - TWO WAY "AND" NPN ONE LOAD				-62	115599					
DESIGN			MODEL	SMS							
DETAIL	RQ	3-1-62	SCALE	NONE							
CHECK	WH	3-1-62	DRAW	LIG 3-17-62							
APPRO			CHECK								

729825

C