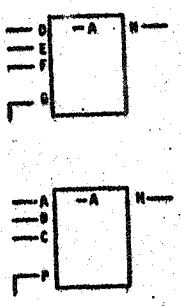
729829

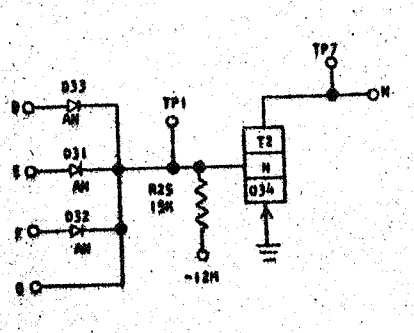
CARD CODE 729829
CJ WF

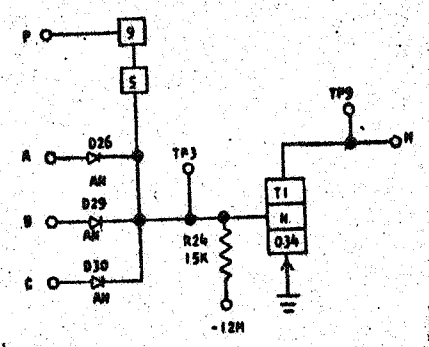
REFERENCE DRAWING

SEE PRODUCTION DRAWING 371268

CTDL 3-WAY "AND" PNP NO LOADS







SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. INPUTS ON EXTENDER CARD DOWN IN COINCIDENCE WITH DOWN INPUTS ON CARD FOR UP OUTPUT
4. COLLECTORS MUST BE LOADED
5. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

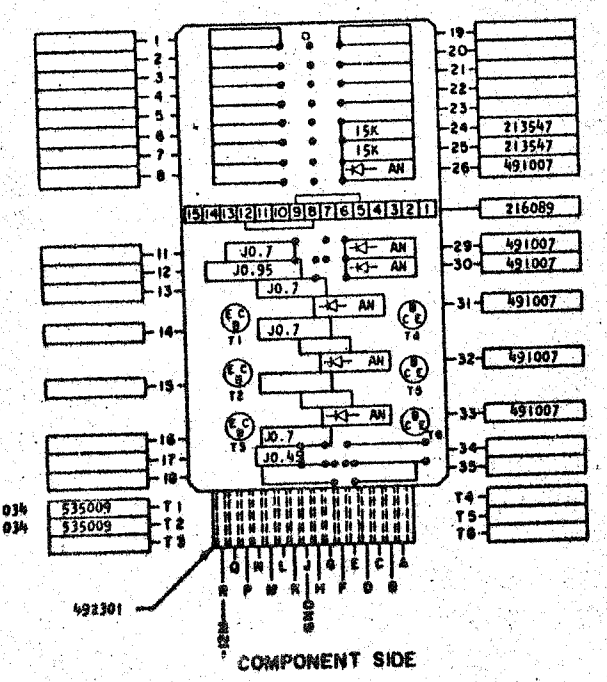
PINS		SIGNAL NAME	WAVE SHAPE	LEVELS	MIN	MAX
D, A	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
E, B	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
F, C	T	INPUT		UP	1.44	6.24
				DOWN	-0.74	-6.24
G, P		EXTENDER INPUT		UP	+6.0	
				DOWN	0.0	
H, N	U	OUTPUT		UP	-0.54	0.24
				DOWN	-7.44	-12.5

DELAY - USEC

	MINIMUM	MAXIMUM
TURN ON	0.10	0.60
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING EF "OR".



CIRCUIT ADD. PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.						DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASH TSTR-CTDL - 3 WAY "AND" PNP NO LOADS					6-29-62	EC 115599					729829
DESIGN				MODEL	SMS	30-4-63	TT 83687					
DETAIL	RB	3-1-62		SCALE	NONE							
CHECK	WF	3-1-62		DRAW	LIG	3-17-6						
APPRD				CHECK								

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