

729871

STANDARD CODE

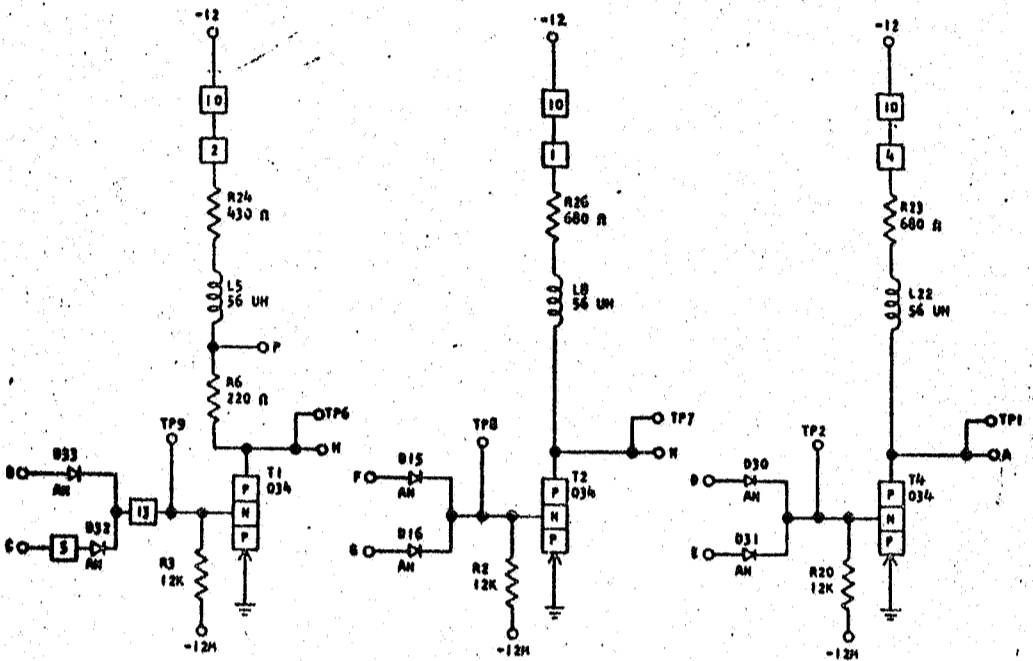
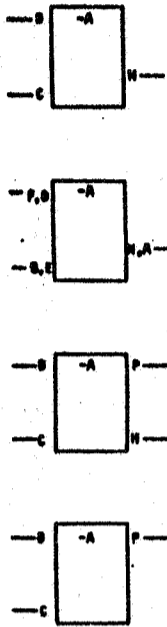
CARD CODE 729871

JG WW

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371580

CTDL HIGH SPEED-TWO WAY "AND" PNP ALL LOADS



SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, TRANSISTOR ON, THE OUTPUT IS UP
3. PIN P IS CURRENT MODE OUTPUT
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

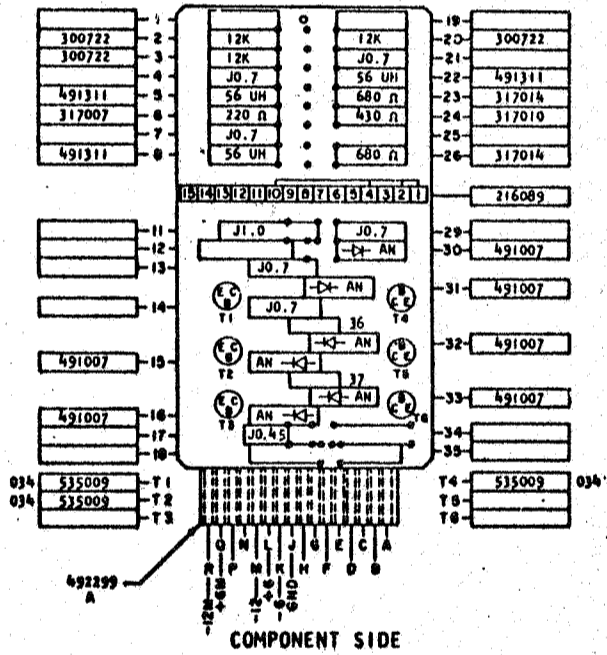
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
B, C	Y INPUT	[Waveform: High then Low]	UP	+1.44 +6.24
			DOWN	-.74 -6.24
H	U OUTPUT	[Waveform: High then Low]	UP	-.54 +.24
			DOWN	-7.44 -12.48
P	P OUTPUT	[Waveform: High then Low]	UP	-4.93 -3.54
			DOWN	-8.82 -12.48
F, D, G, E	T INPUT	[Waveform: High then Low]	UP	+1.44 +6.24
			DOWN	-.74 -6.24
A, N	U OUTPUT	[Waveform: High then Low]	UP	-.54 +.24
			DOWN	-7.44 -12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING OF "ON".



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASH TSTR-CTDL HIGH	DATE	4-27-62	EC	115599					729871
DESIGN	SPEED-TWO WAY "AND" PNP ALL LBS	DATE	30-4-63	ST	83687					
DETAIL	RD 3-1-62	SCALE	NONE							
CHECK	WH 3-1-62	DRAW	LIG 3-17-62							
APPROV		CHECK								

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