

729868

STANDARD CODE

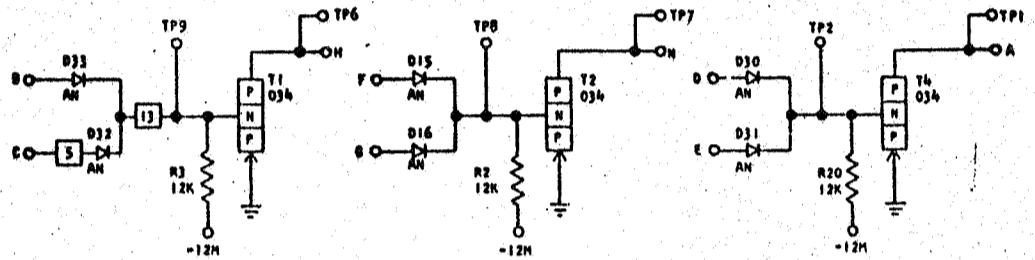
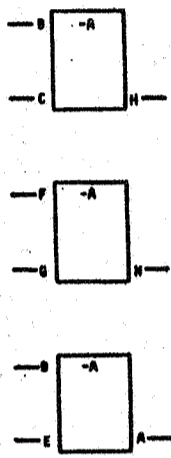
CARD CODE 729868

JG --

REFERENCE DRAWING

SEE PRODUCTION DRAWING 371583

CTDL HIGH SPEED - TWO WAY "AND" PNP NO LOADS



SEQUENCE OF OPERATION

1. ANY INPUT UP, TRANSISTOR IS OFF, THE OUTPUT IS DOWN
2. ALL INPUTS DOWN, THE TRANSISTOR IS ON, THE OUTPUT IS UP
3. ALL OUTPUTS MUST BE COLLECTOR LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN

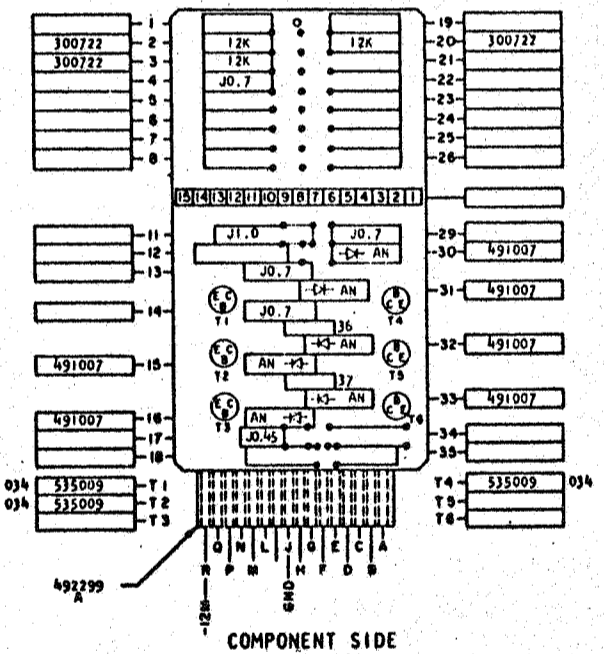
PINS	SIGNAL NAME	WAVE SHAPE	LEVELS	
			MIN	MAX
B, F, D, C, G, E	T INPUT	[Waveform: High level]	UP	+1.44 +6.24
H, I, A	U OUTPUT	[Waveform: Low level]	DOWN	-7.44 -6.24
			UP	-5.44 +2.44
			DOWN	-7.44 -12.48

DELAY

	MINIMUM	MAXIMUM
TURN ON	0.15	0.50
TURN OFF	0.05	0.80*

*THIS DELAY CAN OCCUR ONLY ON HEAVILY LOADED BLOCKS.

NOTE: THE ABOVE RANGES OF DELAYS ARE REPRESENTATIVE. SPECIFIC CIRCUIT APPLICATION AND/OR WIRING CAPACITANCE MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES. IN SUCH CASES, CARD REPLACEMENT SHOULD INDICATE IF THE CIRCUIT IS OUT OF SPECIFICATIONS. EXAMPLE: LOGIC BLOCK DRIVING OF "OR".



COMPONENT SIDE

CIRCUIT AND PACKAGING STANDARDS	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CARD ASM TSTR-CTDL HIGH	DATE	4-29-62	EC	115599					729868
SPEED	TWO WAY "AND" PNP NO LOADS	DATE	30.4-63	JT	83687					
DESIGN	MODEL SMS									
DETAIL	RQ 3-1-62 SCALE NONE									
CHECK	WH 3-1-62 DRAW LTB 3-7-62									
APPROV	CHECK									

729868