729954 | STANDARDS CODE

CARD CODE 729954

SDTDL LOGIC FAMILY DELAY INFORMATION

GENERAL

THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAYS ARE GIVEN ON EACH INDIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIDE. SPECIFIC CIRCUIT APPLICATION AND/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIDED FOR THOSE CASES WHERE CARD REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE DETAILED ANALYSIS IS NECESSARY.

HIGH SPEED, LOW SPEED CIRCUITS

THE SDTDL CIRCUITS ARE CLASSIFIED INTO TWO MAJOR FAMILIES, THE LOW SPEED AND THE HIGH SPEED CIRCUITS. THE DIFFERENCE BETWEEN THE TWO FAMILIES CONSISTS OF THE INPUT SPEED UP CAPACITOR THAT IS USED ONLY IN THE HIGH SPEED LOGIC BLOCKS.

DELAY CHARTS:

NUMEROUS CHARTS GIVING DELAY INFORMATION HAVE BEEN INCLUDED IN THIS DOCUMENT. BOTH MINIMUM AND MAXIMUM DELAYS ARE GIVEN AS A FUNCTION OF SOME VARIABLE OR VARIABLES. NOMINAL DELAYS HAVE BEEN AVOIDED DUE TO POSSIBLE MISINTERPRETATIONS. THE MAXIMUM DELAYS GIVEN ARE SLIGHTLY LESS THAN THE THEORETICAL MAXIMUM DELAY. THE MAXIMUM DELAYS GIVEN SHOULD NOT BE EXCEEDED IN PRACTICAL APPLICATIONS.

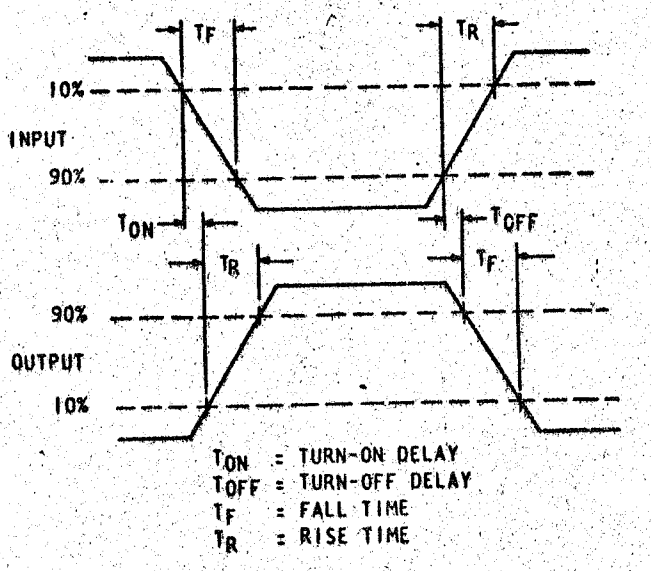
USE OF GRAPHS

THE FOLLOWING STEPS ARE RECOMMENDED FOR USING THE INFORMATION PROVIDED IN THE ACCOMPANYING GRAPHS.

1. GIVEN A LOAD CONFIGURATION REFER TO THE GRAPH OUTPUT FALL TIME VS. LOADING TO DETERMINE THE OUTPUT FALL TIME.
2. GIVEN THE INPUT FALL TIME, THE OUTPUT RISE IS DETERMINED FROM THE GRAPH OF OUTPUT RISE TIME VS. INPUT FALL TIME.
3. KNOWLEDGE OF THE RISE TIME AND USE OF THE GRAPH OF TURN-OFF DELAY VS. INPUT RISE TIME RESULTS IN TURN-OFF LIMITS.
4. KNOWLEDGE OF INPUT FALL TIME AND USE OF THE GRAPH OF TURN-ON DELAY VS. INPUT FALL TIME RESULTS IN TURN-ON LIMITS.

DEFINITIONS

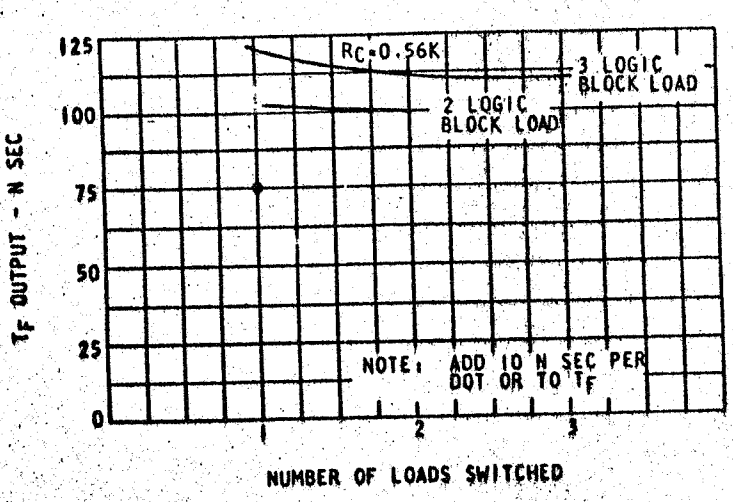
THE RISE AND FALL TIMES WERE MEASURED FROM THE 10% TO 90% POINTS OF THE INPUT AND OUTPUT WAVEFORM. THE TURN-ON DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% DOWN AT THE INPUT TO 10% UP AT THE OUTPUT. THE TURN-OFF DELAY WAS MEASURED AS THE TIME INTERVAL BETWEEN 10% UP AT THE INPUT TO 10% DOWN AT THE OUTPUT. UNLESS OTHERWISE STATED THE RISE, FALL AND DELAY TIMES ARE GIVEN IN N SEC (NANOSECONDS).



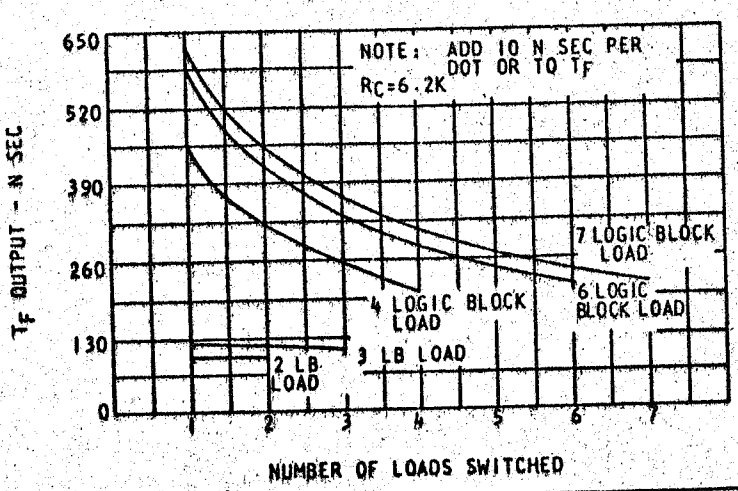
T_{ON} = TURN-ON DELAY
T_{OFF} = TURN-OFF DELAY
T_F = FALL TIME
T_R = RISE TIME

HIGH SPEED SINGLE LEVEL LOGIC BLOCK

OUTPUT FALL TIME VS LOADING



OUTPUT FALL TIME VS LOADING



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME SDTDL LOGIC DELAY INFO. - REF. Dwg				6-11-62	EC115599					729954
				10.4.63	ITB3687					
DESIGN			MODEL							
DETAIL	WDL	3-1-62	SCALE							
CHECK	RG	3-1-62	DRAW							
APPRD			CHECK							

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CARD CODE 729954

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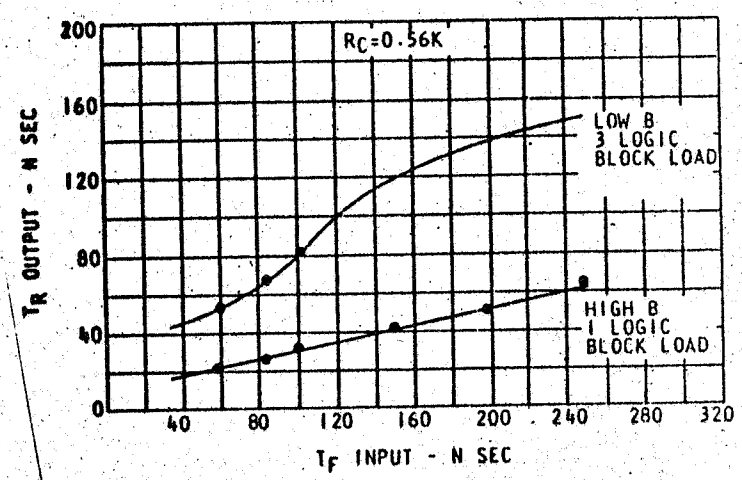
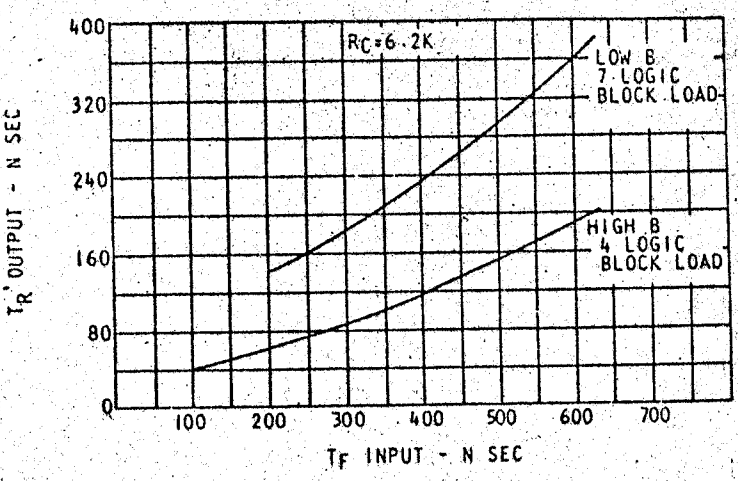
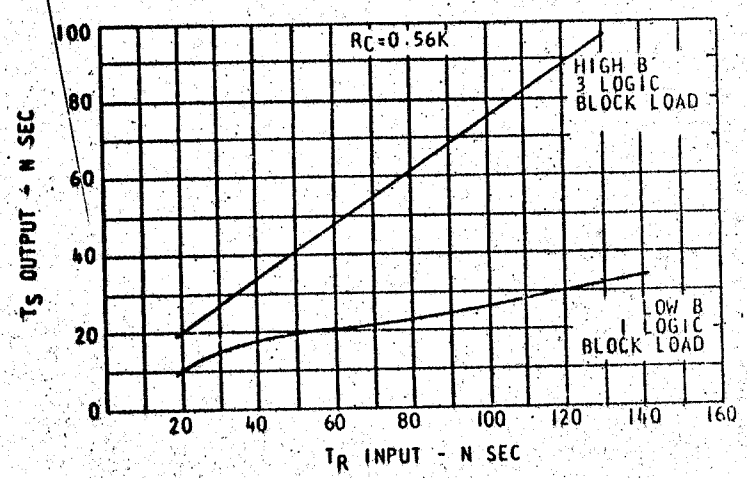
OUTPUT RISE TIME VS INPUT FALL TIME



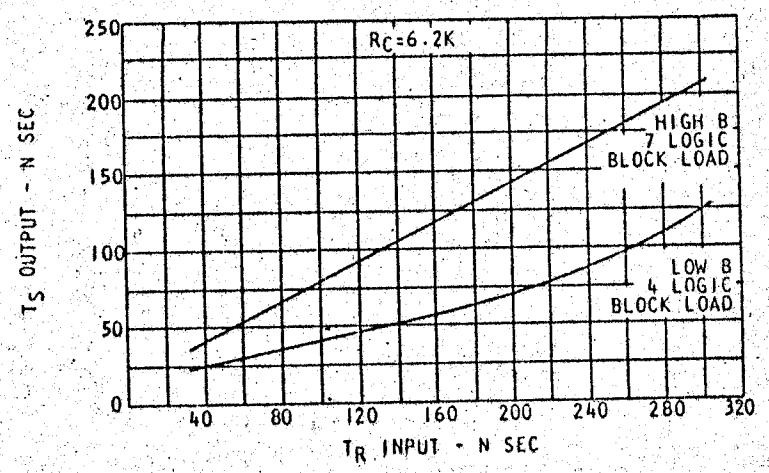
OUTPUT RISE TIME VS INPUT FALL TIME



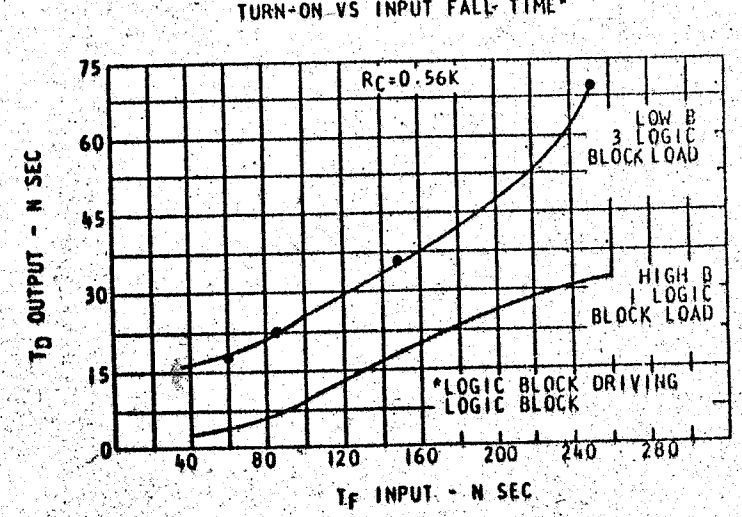
TURN-OFF VS INPUT RISE TIME



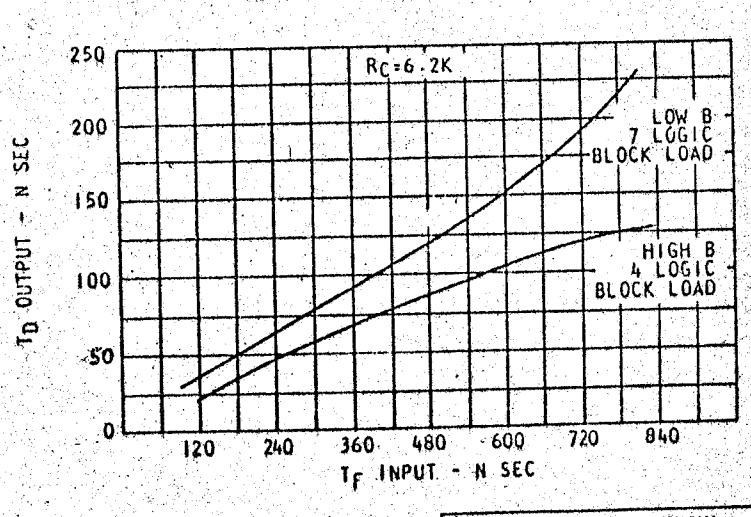
TURN-ON VS INPUT FALL TIME*



TURN-ON VS INPUT FALL TIME



TURN-OFF VS INPUT FALL TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME SDTL Logic Penny				30.4.63	EC 115593					
2 NEG. - REC PULS				30.4.63	TT 83687					
DESIGN			MODEL							
DETAIL	WH	3-1-62	SCALE							
CHECK	RG	3-1-62	DRAW							
APPRD			CHECK							

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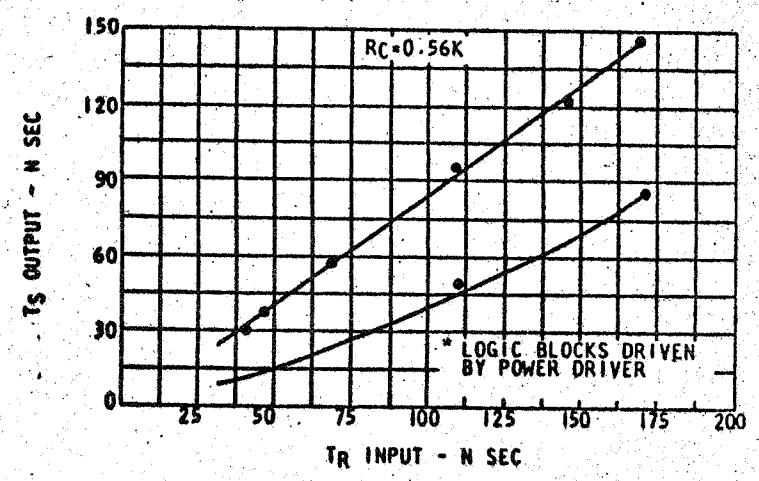
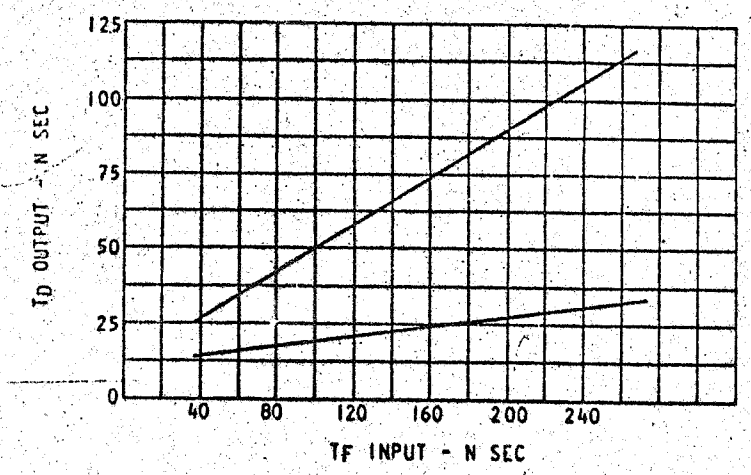
TURN-OFF VS RISE TIME INPUT*



TURN-ON VS FALL TIME INPUT (LOGIC BLOCK DRIVEN BY POWER DRIVERS)



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO	APPROVAL	DEVELOPMENT NO.
NAME	SDTDL LOGIC DELAY				4-11-62	FC115599					
INFO - REF DWG.					30.4.62	TT83687					
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RG	3-1-62	DRAW								
APPRO			CHECK								

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CARD CODE 729954

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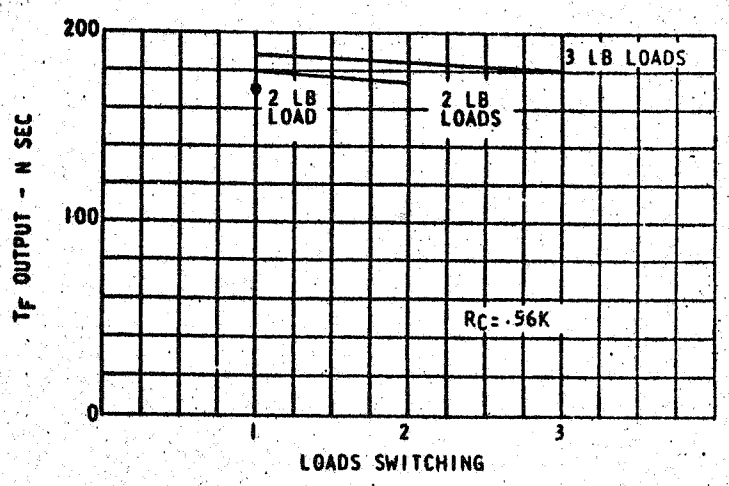
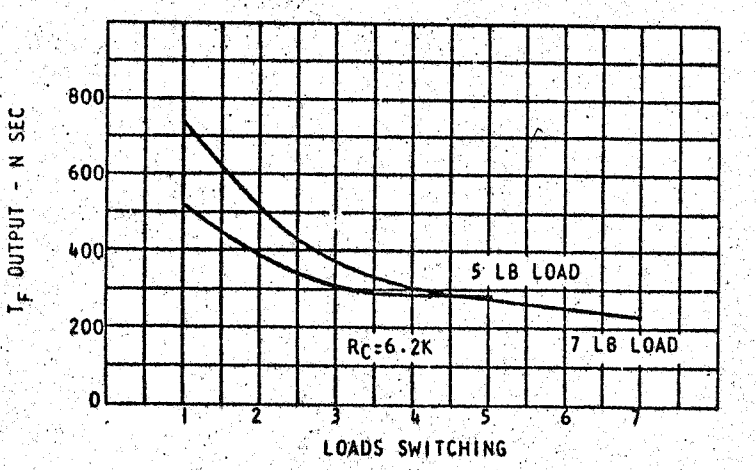
LOW SPEED SINGLE LEVEL LOGIC BLOCKS

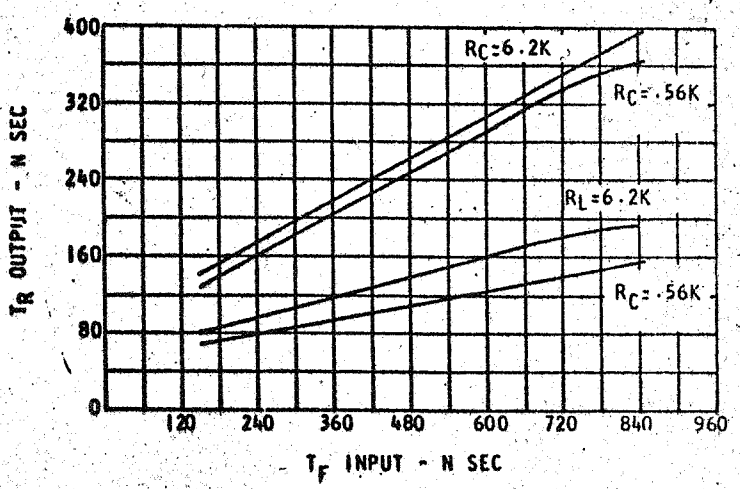
FALL TIME VS LOADING



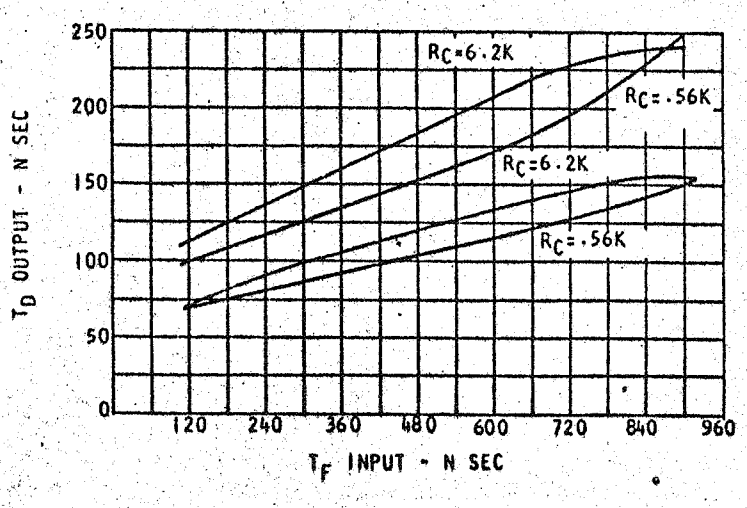
FALL TIME VS LOADING



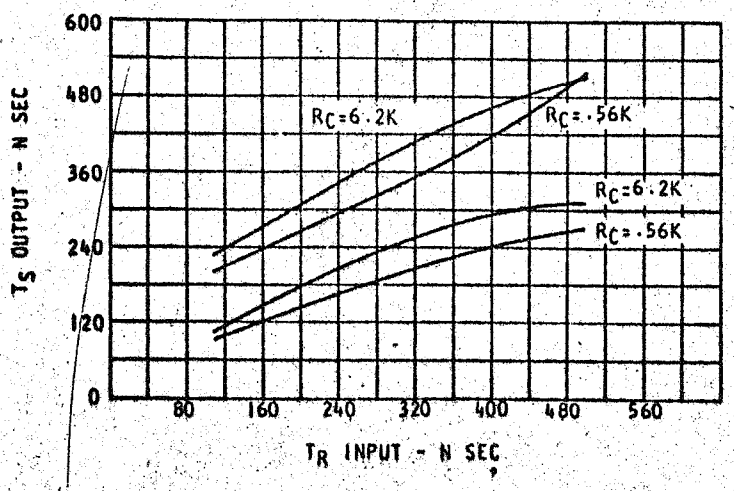
OUTPUT RISE TIME VS INPUT FALL TIME



TURN-OFF VS INPUT FALL TIME



TURN-OFF VS INPUT RISE TIME



CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME SDTDL LOGIC DELAY					-62	EC 115599					729954
INFO. - REF DWG					30.463	JT 83687					
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RQ	3-1-62	DRAW								
APPRO			CHECK								

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