729955

STANDARDS CODE

CTDL DELAY INFORMATION

CARD CODE 729955

SHEET 1 OF 3

GENERAL

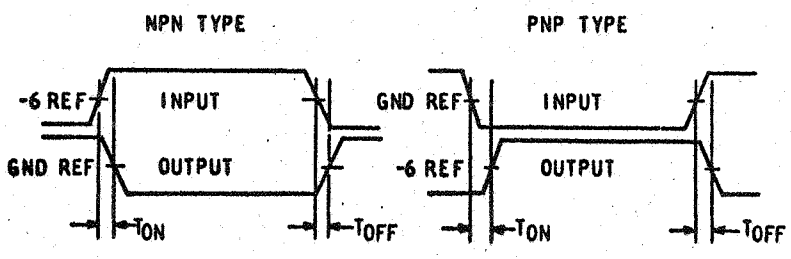
THE TURN ON, TURN OFF DELAYS OF THE CIRCUITS USED IN A PARTICULAR MACHINE ARE COMPLEX FUNCTIONS OF MANY VARIABLES SUCH AS THE TRANSISTOR DELAY, INPUT-OUTPUT LOADING, FALL AND RISE TIME, ETC.

THE DELAY SPECIFICATIONS ARE GIVEN BELOW AND ARE CLASSIFIED BY CIRCUIT TYPE.

WHEN POSSIBLE, REPRESENTATIVE RANGES OF DELAY ARE GIVEN ON EACH INDIVIDUAL CIRCUIT SHEET AND SHOULD BE USED AS A GUIDE. SPECIFIC CIRCUIT APPLICATION AND/OR CAPACITIVE LOAD (EXAMPLE: WIRE CAPACITANCE) MAY RESULT IN DELAYS WHICH ARE OUT OF THE GIVEN RANGES.

THE FOLLOWING INFORMATION IS PROVIDED FOR THOSE CASES WHERE CARD REPLACEMENT DOES NOT RESULT IN IMPROVEMENT AND A MORE DETAILED ANALYSIS IS NECESSARY.

THE DELAY OF THE SIGNAL IN THE CTDL BLOCKS IS A FUNCTION OF THE TRANSISTOR DELAYS PLUS THE LOADING EFFECTS OF THE INPUT AND OUTPUT CIRCUITS. DELAYS FOR SEVERAL STAGES IN CASCADE ARE NUMERICALLY EQUAL TO THE SUM OF INDIVIDUAL STAGES. UNLESS OTHERWISE STATED, DELAYS ARE MEASURED FROM THE TIME THE INPUT SIGNAL CROSSES ITS REFERENCE VOLTAGE TO THE TIME THE OUTPUT SIGNAL CROSSES ITS REFERENCE VOLTAGE, AS SHOWN.



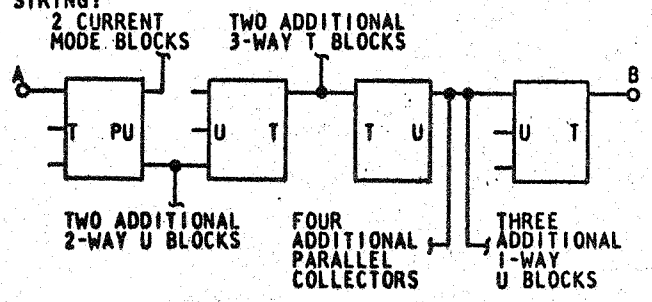
BASIC LOGIC BLOCK DELAY INFORMATION

DATA FOR CALCULATION OF DELAY IN A STRING OF LOGIC WHEN DRIVING CTDL BLOCKS FROM THE CTDL OUTPUT AND CURRENT MODE BLOCKS FROM THE CURRENT MODE OUTPUT.

	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX	MIN	MAX	MIN
DELAY PER PNP BLOCK IN STRING	.70	.20	.18	.06
DELAY PER NPN BLOCK IN STRING	.52	.18	.12	.05
ADDITIONAL DELAY ON STRING				
FOR THE FIRST PNP TYPE LOAD	.00	-.03	.22	.06
FOR THE SECOND PNP TYPE LOAD	.00	-.03	.30	.07
FOR THE THIRD PNP TYPE LOAD	.00	-.03	.40	.08
FOR THE FOURTH PNP TYPE LOAD	.00	-.03	.50	.10
FOR THE FIRST NPN TYPE LOAD	-.01	-.03	.09	.01
FOR THE SECOND NPN TYPE LOAD	-.01	-.03	.13	.02
FOR THE THIRD NPN TYPE LOAD	-.01	-.03	.18	.03
FOR THE FOURTH NPN TYPE LOAD	-.01	-.03	.22	.04
DELAY PER PNP TYPE CS LOADS ON STRING	.02	.00	.02	.005
DELAY PER NPN TYPE CS LOADS ON STRING	.015	.00	.02	.005
DELAY PER PARALLEL COLLECTOR	.007	.00	.01	.004
DELAY PER DIODE INPUT	*.02	.00	.005	.000
DELAY PER 100 PF	.05	.02	.06	.03

* WIRES ASSUMED ON GATES -- INCLUDES WIRING CAPACITANCE EFFECT BETWEEN ADJACENT CARDS.

EXAMPLE OF CTDL DELAY LOGIC STRING. CONSIDER THE FOLLOWING LOGIC STRING:



IN THIS EXAMPLE ALL MAXIMUM DELAYS WILL BE USED:

TURN ON DELAY

2 T BLOCKS	2 X 0.7	= 1.4
2 U BLOCKS	2 X 0.52	= 1.04
5 ADDITIONAL U BLOCKS	5 X(-0.01)	= -0.05
2 ADDITIONAL T BLOCKS	0	= 0
2 P-TYPE CS BLOCK	2 X 0.015	= 0.03
4 PARALLEL COLLECTORS	4 X 0.007	= 0.028
23 INPUT DIODES	23 X 0.02	= 0.46
TOTAL TURN ON DELAY FROM A TO B		2.908 U SEC

TURN OFF DELAY

2 T BLOCKS	2 X 0.18	= 0.36
2 U BLOCKS	2 X 0.12	= 0.24
2 IST U BLOCK LOAD	2 X 0.09	= 0.18
2 2ND U BLOCK LOAD	2 X 0.13	= 0.26
1 3RD U BLOCK LOAD	0.18	= 0.18
1 IST T BLOCK LOAD	0.22	= 0.22
1 2ND T BLOCK LOAD	0.30	= 0.30
2 P-TYPE CS BLOCK	2 X 0.02	= 0.04
4 PARALLEL COLLECTORS	4 X 0.01	= 0.04
23 INPUT DIODES	23 X 0.005	= 0.115
TOTAL TURN OFF DELAY FROM A TO B		1.935 U SEC

LOGIC INVERTER

	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX	MIN	MAX	MIN
DELAY PER PNP INVERTER IN STRING	-.08	-.14	.55	.06
DELAY PER NPN INVERTER IN STRING	0	+.06	.41	-.02
ADDER LOGIC INVERTER DELAY:				
PER PNP INPUT LOAD	0	0	.015	.01
PER PNP OUTPUT LOAD	0	-.005	.01	.006
PER NPN INPUT LOAD	-.02	-.01	.04	.02
PER NPN OUTPUT LOAD	0	0	.01	0
DELAY ACROSS PNP BLOCK DRIVING LOGIC INVERTER IN STRING	.81	.26	.30	.26
DELAY ACROSS NPN BLOCK DRIVING LOGIC INVERTER IN STRING	.38	.28	.20	.14
ADDITIONAL DRIVING BLOCK DELAY				
PER PNP INPUT LOAD	0	0	0	0
PER PNP OUTPUT LOAD	0	-.02	.01	0
PER NPN INPUT LOAD	0	0	0	0
PER NPN OUTPUT LOAD	-.013	-.043	.01	.01
DELAY ACROSS PNP BLOCK DRIVEN BY LOGIC INVERTER	.74	.32	.22	.20
ADDITIONAL DELAY DUE TO INVERTER OUTPUT LOADING				
1ST PNP BLOCK	0	0	.16	.07
2ND PNP BLOCK	0	-.02	.22	.08
3RD PNP BLOCK	0	-.02	.33	.09
4TH PNP BLOCK	0	-.01	.39	.11
DELAY ACROSS NPN BLOCK DRIVEN BY LOGIC INVERTER	.35	.28	.17	.09
ADDITIONAL DELAY DUE TO INVERTER OUTPUT LOADING				
1ST NPN BLOCK	-.02	-.02	.18	.08
2ND NPN BLOCK	-.01	-.01	.21	.10
3RD NPN BLOCK	-.01	-.02	.22	.10
4TH NPN BLOCK	-.01	-.02	.42	.15

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
ABC	4-2-62

INTERNATIONAL BUSINESS MACHINES CORP.				DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. - REF. DWG.			6-29-62	EC 115599					729955
DESIGN			MODEL	30.4-63	JT83687					
DETAIL	WH	3-1-62	SCALE							
CHECK	RO	3-1-62	DRAW							
APPRO			CHECK							

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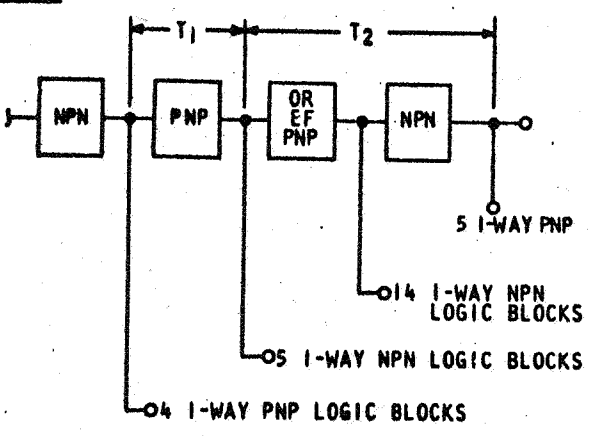
729955 CARD CODE

E, F "OR" CIRCUITS

DELAY INFORMATION

TEST CIRCUIT



PNP EMITTER "OR" DELAY (U SEC)

	T_1 T_{ON} MAX.	T_1 T_{ON} MIN.	T_1 T_{OFF} MAX.	T_1 T_{OFF} MIN.	T_2 T_{ON} MAX.	T_2 T_{ON} MIN.	T_2 T_{OFF} MAX.	T_2 T_{OFF} MIN.
DELAY PER BLOCK	.92	.28	.15	.10	.50	.12	.12	.12
DELAY PER ADDED BLOCK ON DRIVER INPUT	.00	.00	.06	.03	.00	.01	.02	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER OUTPUT	.00	-.01	.00	.00	.01	-.02	.04	.06
DELAY PER ADDED CTDL BLOCK ON E.F.	.01	-.008	.00	.00	.00	-.01	.006	.01
DELAY PER ADDED CTDL BLOCK ON DRIVER BLOCK	.01	.00	.00	.00	-.03	-.01	.00	.00
DELAY W/3 E.F. ON DRIVER - NO LOAD R IN DRIVER	.29	.28	.30	.10	.50	.25	.24	.12
DELAY PER ADDED E.F.	.00	-.02	.02	.00	.00	.00	-.01	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER INPUT	.00	-.01	.02	.00	.00	-.005	-.005	.00
DELAY PER ADDED BLOCK ON E.F. OUTPUT	.00	.002	.002	.00	.00	-.01	.015	.00
DELAY PER ADDED BLOCK ON DRIVER BLOCK	.00	.00	.004	.00	.00	-.02	.00	.00

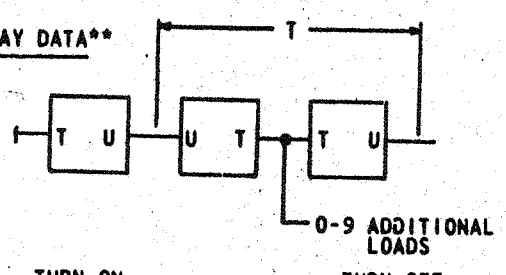
NPN EMITTER "OR" DELAY (U SEC)

	T_1 T_{ON} MAX.	T_1 T_{ON} MIN.	T_1 T_{OFF} MAX.	T_1 T_{OFF} MIN.	T_2 T_{ON} MAX.	T_2 T_{ON} MIN.	T_2 T_{OFF} MAX.	T_2 T_{OFF} MIN.
DELAY PER BLOCK	.42	.36	.15	.14	.70	.19	.10	.06
DELAY PER ADDED BLOCK ON DRIVER	-.02	.01	.05	.08	.00	.00	.01	.02
DELAY PER ADDED CTDL BLOCK ON DRIVER OUTPUT	-.01	-.01	.005	.00	.00	.00	.03	.01
DELAY FER ADDED CTDL BLOCK ON E.F.	.00	.00	.00	.00	.00	.002	.005	.005

	T_{ON} MAX.	T_{ON} MIN.	T_{OFF} MAX.	T_{OFF} MIN.	T_{ON} MAX.	T_{ON} MIN.	T_{OFF} MAX.	T_{OFF} MIN.
DELAY PER ADDED CTDL BLOCK ON DRIVER BLOCK	.00	.00	.00	.00	-.04	.00	.00	.00
DELAY W/3 E.F. ON DRIVER - NO LOAD R IN DRIVER	.32	.36	.15	.14	.70	.20	.16	.06
DELAY PER ADDED E.F.	.02	.00	-.02	.00	.00	.00	.00	.00
DELAY PER ADDED CTDL BLOCK ON DRIVER INPUT	.00	-.02	.02	.00	.00	.00	.01	.00
DELAY PER ADDED BLOCK ON E.F. OUTPUT	.005	.00	.00	.00	-.005	.00	.01	.00
DELAY PER ADDED BLOCK ON DRIVER BLOCK	.01	.00	.00	.00	-.01	-.00	.00	.00

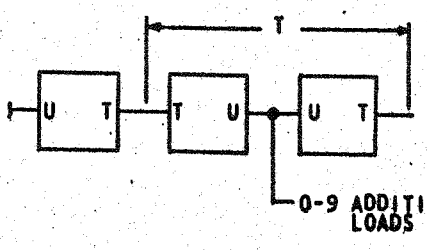
TRANSLATE BLOCK DELAY DATA

NPN BLOCK



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
1	.70	.16	.34	.12
2	.70	.16	.36	.13
3	.70	.16	.40	.14
4	.70	.17	.43	.15
5	.70	.17	.46	.16
6	.70	.18	.48	.17
7	.70	.18	.50	.18
8	.70	.18	.51	.19
9	.70	.19	.57	.20
10	.70	.20	.60	.21

PNP BLOCK



TOTAL NUMBER OF LOADS	TURN ON (U SEC) MAX.	TURN ON (U SEC) MIN.	TURN OFF (U SEC) MAX.	TURN OFF (U SEC) MIN.
1	.52	.17	.26	.14
2	.52	.17	.31	.16
3	.52	.17	.35	.17
4	.52	.18	.38	.19
5	.53	.18	.41	.20
6	.53	.18	.44	.21
7	.53	.19	.47	.22
8	.53	.19	.50	.23
9	.53	.19	.54	.24
10	.53	.20	.56	.25

CIRCUIT AND PACKAGING STANDARD	
APPROVAL	DATE
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INTERNATIONAL BUSINESS MACHINES CORP.					DATE	CHANGE NO.	APPROVAL	DATE	CHANGE NO.	APPROVAL	DEVELOPMENT NO.
NAME	CTDL DELAY INFO. - REF. DWG.				6-28-62 30.4.53	FC113599 TT83687					729955
DESIGN			MODEL								
DETAIL	WH	3-1-62	SCALE								
CHECK	RG	3-1-62	DRAW								
APPRO			CHECK								

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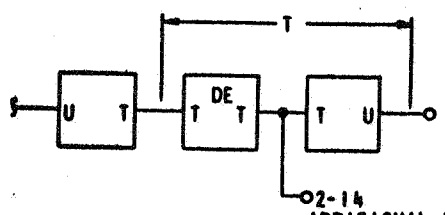
CARD CODE 729955

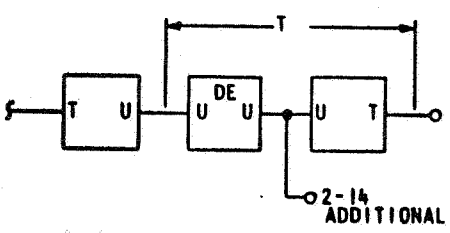
EMITTER FOLLOWER DELAY

NPN



TOTAL NUMBER OF LOADS	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX.	MIN.	MAX.	MIN.
3	.68	.14	.25	.05
4	.68	.15	.26	.06
5	.68	.16	.27	.06
6	.68	.17	.27	.07
7	.68	.18	.29	.07
8	.68	.19	.30	.08
9	.68	.20	.31	.08
10	.68	.21	.32	.08
11	.68	.21	.33	.08
12	.68	.21	.34	.08
13	.68	.22	.35	.09
14	.68	.22	.36	.09
15	.68	.23	.37	.09

PNP



TOTAL NUMBER OF LOADS	TURN ON (U SEC)		TURN OFF (U SEC)	
	MAX.	MIN.	MAX.	MIN.
3	.48	.18	.17	.06
4	.50	.19	.18	.06
5	.52	.20	.19	.07
6	.54	.21	.21	.07
7	.56	.22	.22	.08
8	.58	.23	.23	.08
9	.59	.24	.24	.09
10	.59	.24	.26	.09
11	.60	.25	.28	.09
12	.60	.26	.29	.10
13	.61	.26	.30	.10
14	.61	.27	.31	.10
15	.62	.27	.33	.10

CURRENT MODE BLOCK WITH CTDL COUPLING NETWORK

DELAY DATA

	TURN ON (U SEC) IN PHASE MIN	IN PHASE MAX	INVERTED MIN	INVERTED MAX
BASIC N BLOCK DELAY	.100	.100	.150	.200
PER CTDL BLOCK LOAD	-.010	-.005	-.020	-.005
PER ADDED FAN-IN DIODE	-.002	-.002	-.001	-.001
BASIC P BLOCK DELAY	.080	.110	.210	.240
PER CTDL BLOCK LOAD	.000	.010	-.020	-.005
PER ADDED FAN-IN DIODE	-.001	-.001	-.002	-.002
BASIC CTDL PNP DELAY	.230	.560	.200	.500
PER CTDL BLOCK LOAD	.000	.020	.000	.020
PER ADDED FAN-IN DIODE	-.020	-.020	-.022	-.012
BASIC CTDL NPN DELAY	.200	.450	.180	.400
PER CTDL BLOCK LOAD	.020	.020	-.010	-.010
PER ADDED FAN-IN DIODE	.015	.030	-.018	-.006

	TURN OFF (MU SEC) IN PHASE MIN	IN PHASE MAX	INVERTED MIN	INVERTED MAX
BASIC N BLOCK DELAY	.090	.090	.090	.130
PER CTDL BLOCK LOAD	.010	.010	.010	.010
PER ADDED FAN-IN DIODE	.001	.001	.001	.001
BASIC P BLOCK DELAY	.060	.130	.100	.120
PER CTDL BLOCK LOAD	.000	.020	.010	.010
PER ADDED FAN-IN DIODE	.002	.002	-.001	-.001
BASIC CTDL PNP DELAY	.060	.340	.140	.350
PER CTDL BLOCK LOAD	.020	.100	.000	.100
PER ADDED FAN-IN DIODE	.002	.021	.012	.020
BASIC CTDL NPN DELAY	.160	.220	.140	.170
PER CTDL BLOCK LOAD	.100	.260	.060	.290
PER ADDED FAN-IN DIODE	.005	.010	.005	.010

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NAME	CTDL DELAY INFO. - REF. DWG				6-29-62	EC 115599					729955
					30.4.63	JT 83687					
DESIGN			MODEL								
DETAIL	WM	3-1-62	SCALE								
CHECK	RG	3-1-62	DRAW								
APPRD			CHECK								

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