

The Functional Explanation: The Half-Executed Branch

To the software developer, the Halt and Branch instruction (. iii) appears to execute as a single atomic unit. However, the IBM 1401 CPU splits this execution into distinct phases:

1. **Instruction Fetch (I-Phase):** The Op-code . is read, and the 3-character branch target address (iii) is moved into the **B-Address Register (B-AR)**.
2. **Execution Phase (E-Phase):** The machine enters an E-phase solely to execute the “Halt” portion. The **Stop Latch** is tripped, immediately cutting the system clock and halting the machine before the program counter updates.
3. **The Trap:** At this moment of stagnation, the next sequential instruction address is still safely held in the **I-Address Register (I-AR)**, while the branch target is held in the **B-Address Register (B-AR)**. The hardware has not yet copied the B-AR over to the I-AR to finalize the branch step.

If you simply press **Start**, the machine picks up exactly where it left off, moving the B-AR contents into the I-AR and executing the branch.

However, if you press **Start Reset** first, it overrides the control latches. It forces the internal state machine out of the branch-execution loop and resets the memory cycles. Because the I-AR still points to the instruction immediately following the halt, pressing **Start** next forces the machine to fetch from the current I-AR, bypassing the branch target trapped in the B-AR.

The ALD Circuit Analysis

You can trace exactly how the **Start Reset** key kills the impending branch by focusing on the logic gates controlling the **Instruction Ring (I-Ring)** and the **Address Register Gate Controls**.

1. The Branch-Execution Loop

- **ALD Block 15.10.xx to 15.38.xx (I-Control / Op Decoding):**

When the . Op-code is decoded alongside an address, it sets the Halt and Branch state. The hardware triggers a specific latch: +S OP DECODE HALT BR.

- **ALD Block 31.32.11.2 (Process Stop / Halt Controls):**

This latch immediately sets the Process Stop Latch. When this latch drops, it suppresses the main +S CLOCK DRIVE signal. The machine freezes at the end of the current instruction read cycle, preventing the internal transfer gate (B-AR to I-AR Transfer) from firing.

2. The Start Reset Clearing Mechanism

- **ALD Block 31.30.11.2 (Console Reset Lines):**

Pressing the physical Start Reset key sends a -S START RESET KEY pulse down the main reset rail.

- **ALD Block 31.32.11.2 & 15.10.12.1 (Ring Reset):**

This reset line branches directly into the clear inputs of the instruction sequencing rings. Crucially, the START RESET signal sends a DC-reset pulse to the branch control latches, dropping -S OP DECODE HALT BR.

- **The Fatal Bypass:**

Because the branch latch is forcibly cleared while the clock is stopped, the hardware "forgets" that it was in the middle of a branch sequence.

- **ALD Block 14.10.31.2 (Address Register Gating):**

When you subsequently press the physical Start key, the machine initiates a standard instruction-fetch cycle (I-Phase 1). Because the HALT BR modifier is gone, the gate that causes B-AR → I-AR transfer never receives its activating pulse. The machine defaults to reading memory from whatever address is currently sitting inside the I-Address Register (I-AR) — which is the next sequential instruction.

Where It Was Documented

Because this was technically an emergent property of the console reset logic rather than an officially designed software feature, you will not find it in the primary sections of the IBM 1401 Principles of Operation.

Instead, this behavior was cataloged in two obscure places:

1. **IBM Customer Engineering (CE) Instructional Manuals:** Specifically, the Instruction Logic or Console Controls supplemental training guides for field engineers. These manuals detailed exactly what every console key reset at the flip-flop level to help technicians diagnose sticking latches.
2. **Distribution Utility Program READMEs:** The operating instructions for the specific IBM Tape-to-Card/Card-to-Tape distribution program (such as the 1401-UT-026 or 1401-UT-041 system utilities) featured a "Program Halts" table. In the notes section for the configuration halts, it explicitly told the operator: *"To select Option A, press START. To select Option B (if sense switches are not installed), press START RESET then START."*

Bob Supnik drew my attention to A24-3067-2, which is generously larded with change bars. It documents this behavior on page B-34.